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SIMULATION BASED CAUSE AND EFFECT ANALYSIS OF CYCLE TIME DISTRIBUTION IN SEMICONDUCTOR BACKEND

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ABSTRACT

We analyzed the effect of a number of controllable input parameters on cycle time distribution and other output variables in a complex semiconductor backend manufacturing system, using a data driven, discrete event simulation model. A validated model was used as the base case and the effects were quantified against the base model to analyze the relative merits and sensitivity of each of these input variables. Input variables that are analyzed include lot release controls, heuristic scheduling rules, machine up time, setup time, material handling time, product flow, and lot size. We have used actual data from a major semiconductor back-end site for our analysis and showed the impact of lot release scheduling on cycle time distribution.

1 INTRODUCTION

Intense competition and supply chain management drives have resulted in semiconductor manufacturers to initiate programs to improve their market responsiveness by reducing the cycle time whilst narrowing the cycle time distribution to achieve greater repeatability. We used a validated discrete event simulation model to analyze the cause and effect of the semiconductor back-end manufacturing system. In particular we analyzed the effect of a number of controllable input variables on selected output variables of cycle time distribution and throughput.

Figure 1 shows our focus. The research was initiated with a vision to resolve the issue of wide cycle time distribution in semiconductor back-end and this research has contributed towards achieving significant impact on cycle time distribution reported earlier in Sivakumar 1999.

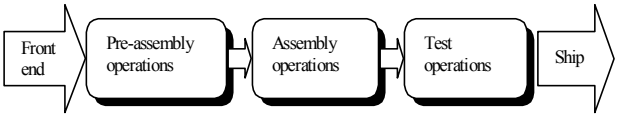

Figure 1: Semiconductor Backend

We define lot cycle time as the duration from the release time of a lot at the first operation to the time it is packed ready for shipment. A commonly used measure of cycle time spread in semiconductor manufacturing is the 98 percentile (98 %-ile) cycle time. 98 %-ile cycle time may be defined as the lowest cycle time of the 98 % of the lots completed during a specific period of for example, a month.

Live data from a major semiconductor backend site based in Singapore is used for our analysis. The backend site was established during the early seventies and progressively expanded and currently manufactures over 275 million IC's per year. The varieties include PC products, telecommunication, ASIC's, military, aerospace, and many other types of IC's for local as well as overseas markets.

2 SEMICONDUCTOR BACKEND

There are four distinct stages in semiconductor or IC manufacturing and these are wafer fabrication, wafer probe or test, IC packaging and assembly, and IC burn-in and functional (electrical) test. IC assembly, IC burn-in and functional (electrical) test operations are also carried out in the back-end. The focus of this paper is backend operations. In general there is a high variety of products and a typical back end facility may handle of the order of 2000 products, each requiring different route specifications resulting in a substantially high number of process flows or routings. High product mix leads to variations of routing and process time.

Cycle time of the assembly operation in a typical back-end usually falls in the range of 3-6 days. Typical test operation cycle time is in the region of 1.5 to 15 days. One of the primary objectives of the research reported in our paper is to identify the factors that influence this wide cycle time distribution so that we can attempt to reduce the cycle time and its distribution.

3 ANALYSIS METHODOLOGY

Substantial research has been reported relating to simulation based analysis (Mazziotti and Horne 1997, Morito and Lee 1997). The simulator mimics the behavior of the actual system in an intuitive manner that enables the users to understand the logic (Hopp and Spearman 2000) and this is one of the major advantages of discrete event simulation. Off line analysis of semiconductor front end has been widely reported (Rose 1998, Domaschke et al. 1998).

We constructed the semiconductor backend manufacturing model using AutoMod™ simulator. The model made use of features such as machine definition, product routes and processes, yield, rework, machine units per hour (UPH), batch process time of ovens etc, mean time between failures (MTBF), mean time to repair (MTTR), setup time matrix, and preventive maintenance schedules. Figure 2 shows the scale of the model (Sivakumar 2000).

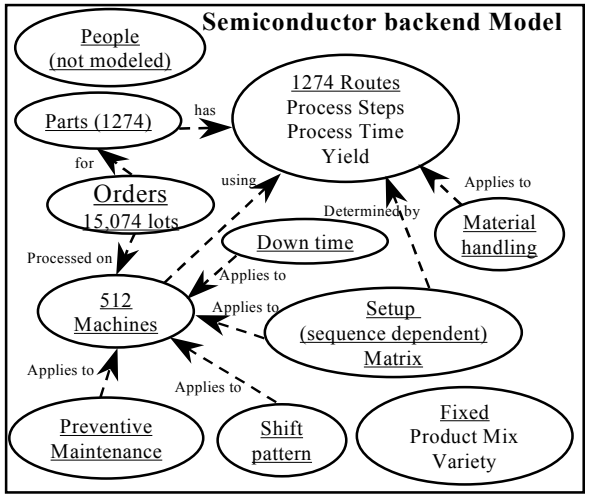

Figure 2: Simulation model of Semiconductor Backend

All the active machines in the factory were modeled and this represents a total of 512 unique machines in 184 station families. A total of 1274 products are modeled with unique routes that defines their sequence of steps they must follow to go from its wafer state to a finished IC assembly state. Process time and yield information and their distribution arguments are also defined. The internal transport and material handling time are also modeled with distribution arguments. Setup matrix is defined with the setup changeover time between two sequence dependant setups.

Sequence of operations on different resources in a factory is controlled by rules (policies). The general rule followed in the actual factory is earliest start date (ESD). The base model is specified with ESD dispatch rule for all operations except lot starts. Lot starts were modeled based on deterministic schedule using actual date and time at which each lot is released in to the first operation.

Machine unavailable times such as shift breaks, down time, and preventive maintenance, are defined in the calendar files. The factory is modeled with all machines (except batch process machines such as ovens) to stop operating during shift, meal and tea breaks. Downtime is modeled with MTBF and MTTR using appropriate distributions arguments. Preventive maintenance (PM) is modeled using actual plans and applied with distributions on the duration of PM time.

We have observed that WIP in the system reached realistic steady levels over a period of 10 days of simulation from zero inventory status. We used the first 14 days as warm-up period and analytical data was captured for the subsequent 28 days. (WIP assignment feature was not available in the AutoMod version we used).

Test machines use a large variety of complex handlers and hardware as reported in Sivakumar (1999) and these are not modeled. Certain test machines have multiple test heads whose co-processing constraints are not modeled. Machine allocations for different product families are fixed for the simulation horizon. The burnin hardware is not modeled and burnin batching policies were simplified. Binning in test area is not modeled. Operators are not modeled in our study. These assumptions had some effect on the model validation.

4 MODEL VERIFICATION AND VALIDATION

The model was verified in a number of iterations starting from simple output checks to complex walkthroughs using flow charts. The model was finally verified using 'trace' technique (Law and Kelton 1991).

We used a 'correlated inspection approach' to model validation (Law and Kelton 1991). As shown in Figure 3, we collected historical data from the actual factory and then compared the model and system output of selected variables after the warm-up period. We used the input data for multiple replications with different random seed number.

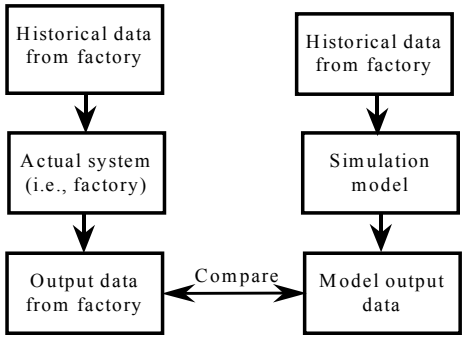

Figure 3: Correlated Inspection Based Validation

In each replication we analyzed a set of output variable with the objective to construct 90 % confidence interval (Sivakumar 2000). We have validated throughput,

cycle time, and WIP levels of three different product groups using the above technique and these are (a) products that leave after assembly process, (b) products only join for test processes and (c) products that are assembled and tested as shown in Figure 4.

Figure 4 shows throughput, 98 %-ile cycle time, and average cycle time of the three product groups for the base model and the system (factory). Start date and time and the quantity of starting lots in the model are identical to that of the system. Figure 4 shows that at the end of the 28 days, the model output of mean throughput of assembled and tested product group is about 7.3% higher than the system throughput. Model output of 98 %-ile cycle time is about 11% higher than the system output, giving an acceptable validation of the model.

5 EXPERIMENTATION

We conducted simulation runs with all three product groups and in this paper we report on the finding relating to the product group of assembly and test products. Figure 5 outlines the input variables that are altered and the model output variables on which the effects were analyzed.

We used the validated model as the base case and quantified the effects against the base model and not the system because we are interested in the relative merits of these input variables.

5.1 Theoretical Cycle (Process) Time

Theoretical cycle time is one of the critical factors affecting the cycle time. We define this as the sum of pure process time of a part number through its entire route based on a fixed lot size. It excludes transport time, material handling time, and queuing time. Reported in this paper is an analysis using 1500 pieces for each unique part number. A segment of the theoretical cycle time distribution and the values are shown in Figure 6. The wide variations in theoretical process time can be seen in Figure 6. The variations are caused by several factors including different lead counts (wire bond operations), different test times / number of test steps (test operations), and packages (mold operations). Variability has been identified as one of the major causes of congestion (Hopp and Spearman 2000) and therefore contributes to a large variation in cycle time distribution and WIP levels.

Theoretical ratio or flow factor is one of the measures used in bench marking competitiveness of operations (Hopp and Spearman 2000). But often a theoretical ratio based on mean theoretical process time is used. In this

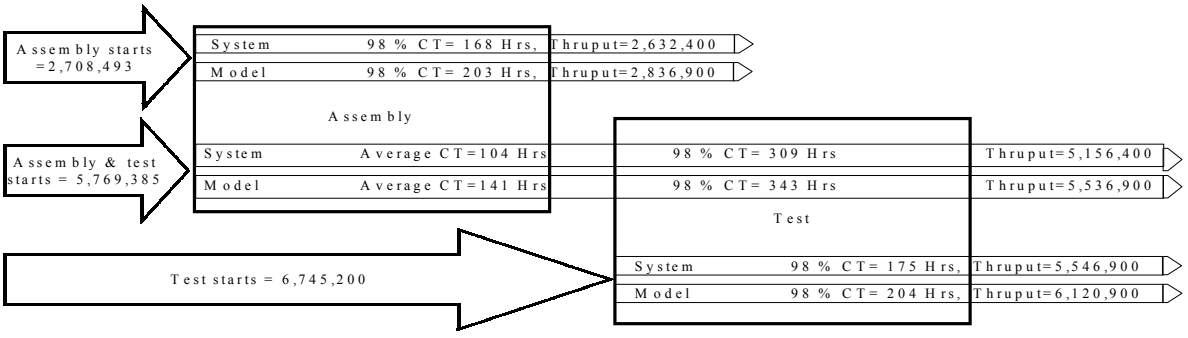

Figure 4: Overall Validation

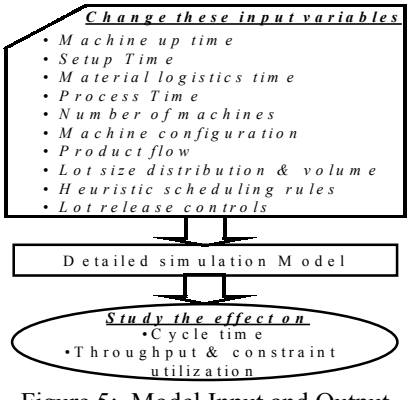

Figure 5: Model Input and Output

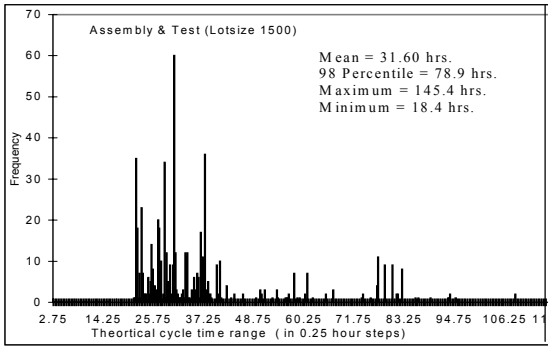

Figure 6: Theoretical Cycle (Process) Time

(Hopp and Spearman 2000). But often a theoretical ratio based on mean theoretical process time is used. In this case the mean theoretical process time is 31.6 hours. The ratio between 98%-ile cycle time and the mean theoretical cycle time is the theoretical ratio of 98%-ile cycle time. Due to the wide distribution to the theoretical process time, theoretical ratio based on mean value may be misleading. However as this ratio is one of the benchmarks, we will continue to refer to this ratio in this paper. Table 1 shows the summary of theoretical cycle time and the mean cycle time predicted by model for assembly and tested product group.

Table 1: Cycle Time Measures in Hours

Cycle time measure	Mean	98%-ile CT
Base model(4048 lots)	141	343
Process time + queue time of base model (4048 lots)	102	291
Theoretical Process time lot qty.=1,500, 1,274 parts	31.6	78.9

The first row is the result of stochastic run of the base model. The second row shows the Process time + queue time of base model. Third row shows the theoretical cycle time of all 1274 parts with a fixed lot size of 1500.

It can be seen from Table 1 that the effect of queuing on the mean cycle time is of the order of 109 hours (141-31.6) or a staggering 77 % and the effect of the same on 98 %-ile cycle time is 264 hours (343 – 78.9) or 77%. On the other hand, the combined effect on the mean cycle time of lot events such as internal material handling, is about 39 hours or 27% of the mean cycle time of 141 hours. The effect of the same on 98 %-ile cycle time is 52 hours or 15% of 343 hours. The process time is the only value adding time and we can conclude that the queuing time component of 98 %-ile cycle time is an overwhelming value of between 3 and 5 times that of all other non value adding time, and a major contributor of cycle time distribution.

5.2 Material Handling, Setup, PM, and Failures

Table 2 shows the effect of material handling, setup, PM / failures and eliminating selected operations.

Table 2: Effect of Machine Failures, PM, & Setup

Change	Mean ct	98%-ile ct	Thruput
Base	100	100	100
No mtl handling time	94.35	98.27	101.09
No setup time	91.59	97.60	103.96
Half MTBPM double MTBF same MTTR	96.29	98.50	102.14
Remove 'Deflash' opertn.	94.5	98.25	102.2
No Deflash & Plating ops.	93.5	97.60	102.56

The respective value of base case is 100, shown in the first row for simpler comparison. The results are mean values of multiple runs. The improvements gained in all these runs are considered marginal, as they are less than 3% on the 98%-ile cycle time and below the validation gap.

5.3 Effect of Lot Size

A thorough lot size analysis would require extended study because lot size distribution is one of the complex variables affecting both cycle time distribution and throughput and is beyond the scope of this paper (Potoradi et al. 1999). In one of our experiments we halved the lot size by assigning two lots with half the base lot size for each lot. In the second experiment we split the lots with quantities smaller or equal to a ceiling set by the factory. Total volume of released lots and the release time and date remained same as the base line in both of these experiments.

Table 3 shows the results of the two lot size runs and, it does appear that with same lot starts, the effect of reducing the lot size on cycle time and throughput was not significant. Setting a lot size ceiling seems to deteriorate mean cycle time with some impact on cycle time spread.

Table 3: Lot Size Effect on Cycle Time

Change	Mean CT	98%-ile CT	Thruput
Base	100	100	100
Half lot size	101.1	99.7	100.6
Lot size ceiling	114.8	102.6	100.5

The mean lot size of the 4048 lots is computed as 1666 and the distribution of the lot quantity of the 4048 lots is shown in Figure 7, indicating a wide distribution.

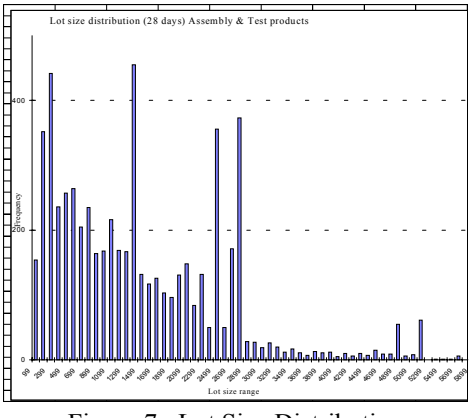

Figure 7: Lot Size Distribution

Although we were unable to detect a distinct pattern in the distribution, individual spikes at certain lot sizes are the preferred lot sizes of high volume products based on the standard dice per wafer quantity.

In a limited analysis similar to that reported in (Hopp and Spearman 2000) we examined the gross effect of lot size on relative cost and average cycle time on a medium volume product of the factory and the results are shown in Figure 8. The cost values are based on the relative costs

identified by the factory. As lot size is increased, the setup time (and setup cost) is reduced at the expense of cycle time translated as stock carrying cost. It can be seen that from an overall point of view, a good operating region for the lot size is between 1500 and 2300. Although the factory data showed that the average lot size is 1666, the distribution is wide resulting in large variations in cycle time, contributing to the 98 %-ile cycle time.

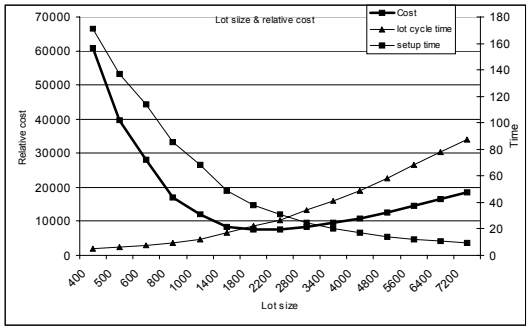

Figure 8: Lot Size Relationship of Cost and Time

Our lot size runs are insufficient to draw any firm conclusions. However it appears that with same lot start volume, the effect of reducing the lot size or setting a lot size ceiling on cycle time distribution is not significant. Quantifying lot size distribution dependency of cycle time distribution requires further research.

5.4 Effect of Heuristic Scheduling Rules

Base simulation run uses earliest start date (ESD) and we have carried out runs to examine three heuristics and these are First in first out (FIFO), Least pieces ahead (LPA or LWNQ), and Same setup (SSU) as shown in Table 4.

Table 4: Effect of Heuristic Machine Scheduling Rules

Change	Mean CT	98%-ile CT	Throughput.
Base (ESD)	100	100	100
FIFO	86.0	117. 9	100.5
LPA (LWNQ)	89.0	104.6	100.8
SSU	81.8	111.6	103.5

The LPA rule is reported in the literature and referred as LWNQ in Wein (1988). Analysis of heuristic scheduling policies is covered in the literature including Lu,, Ramaswamy and Kumar (1994). All three heuristic machine-scheduling rules gave an improvement in mean cycle time at the expense of cycle time spread indicated by the 98 %-ile cycle time. SSU enables improvement in both mean cycle time and throughput at the expense of about 12% increase in cycle time spread.

The experimental runs confirm the reported research including Lu, Ramaswamy and Kumar (1994) that individual machine schedule has an impact on the cycle time spread. Our results also confirm previous results obtained in Wafer FABS (Wein, 1988). Wein, 1988 showed a mean time difference of 4.2% and 3 % in two sets of results between FIFO and LWNQ and this is very close to the results we have obtained of 3.4% (i.e.89 – 86) /86).

5.5 Effect of Start Volumes

We have changed the start volumes by changing the lot sizes by fixed factors of -5%, -10%, -15%, +5%, +10%, and +15% of the original lot quantity, maintaining the original lot release times and examined the effect on cycle time spread. One factor in this run is that it is impossible to avoid the interference of the effect of changing lot size distribution function on the results as this in itself has an effect on cycle time distribution. Figure 9 shows the results.

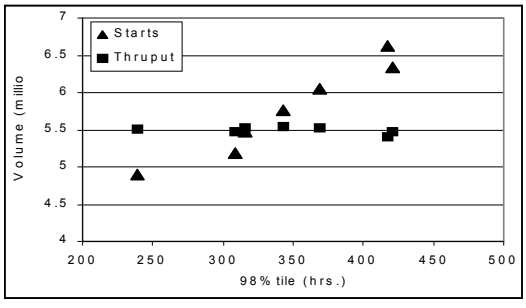

Figure 9: Effect of Volume and Lot Size Reduction

Increasing start volume caused a significant deterioration on cycle times. This series of run showed that increasing the starting quantity does not result in an increased throughput but deteriorates both 98 %-ile and mean cycle times, confirming past research (Hopp and Spearman 2000).

We extended the volume reduction experiment in selectively reducing the start volume by reducing lot size by 15 % for the lots that use any of the 15 most utilized machine families as shown in Table 5. When analyzed in terms of overall volumes, this was found to be equivalent to a 10% reduction in all the lot sizes. Table 5 shows the values together with a comparison line showing the results of 10% overall lot size reduction with base values as 100.

Table 5: Cycle Time Effect of Volume Reduction

Change in lot size	Mean CT	98%-ile CT	Throughput.
Base	100	100	100
-15% reduction of lots that routed through 15 most machine families	64.7	69.6	102.5
-10 % across all lots	68.7	90.0	98.9

As shown in Table 5, significant improvements of 35% and 30% were achieved in mean and 98 %-ile cycle time respectively with a marginal improvement in throughput when lot sizes are reduced selectively.

When 10 % reduction of start volumes is achieved across all products, the cycle time distribution is reduced by 10 % with a loss of 2.5 % throughput. However when the same volume reduction is realized selectively on lots routed through the constraint machines, the cycle time distribution is reduced by 30.4 % with a 1 % improvement in throughput. Several authors including Goldratt and Cox (1986) identified such significance of controlling the constraint machines and this experiment showed that loading of the constraint machine is one of the critical aspects of the cycle time distribution.

6 EFFECT OF LOT RELEASE CONTROL

We analyzed the base lot release schedule that got actually used in the factory during the period of analysis and the daily loading in terms of processing hours were plotted (figure 10).

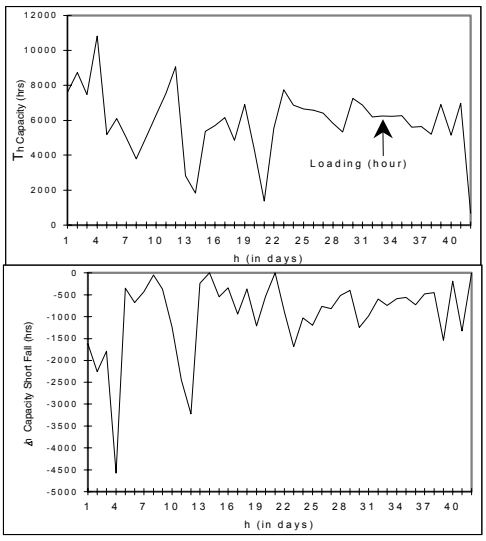

Figure 10: Machine Hours for Daily Released Lots

Required machine station hours in time slot h for all machine work stations m, $m=1,2,...M$ is defined as T_h. The short fall in cumulative machine station hours at time slot h is defined as Δ_h. We examined the actual release of jobs by plotting the values of T_h and Δ_h against time slot h. Figure 14 shows the values of T_h and Δ_h of system lot release.

It is apparent from Figure 10 that the daily processing hour requirements for the released lots were highly variable. There are three aspects to this variation and these are the erratic daily loading, the overloading of available capacity and thirdly the variation of lot quantities.

We carried out runs to analyze the effect of a more uniform lot release and this was achieved by reassigning new release time and date, based on available daily capacity in terms of processing hour requirements on the machines. All 15,078 lots were rescheduled and each lot was reassigned with a new release date and time. No new lots were created. In each day, the new schedule has similar proportion of assembly only lots, test only lots and, assembly and tested lots (see Section 4) to that of the original lot release schedule used by the factory.

We carried out two experiments, one based on lot release to match daily machine capacity and the second schedule is based on 20 % over the available daily machine capacity. Figure 11 shows the demand machine hours of the new daily lot release schedule based on matching daily capacity and, shows almost no capacity short fall (first experiment). As shown, the revised release demands a more uniform daily machine hour compare to that of the original release schedule.

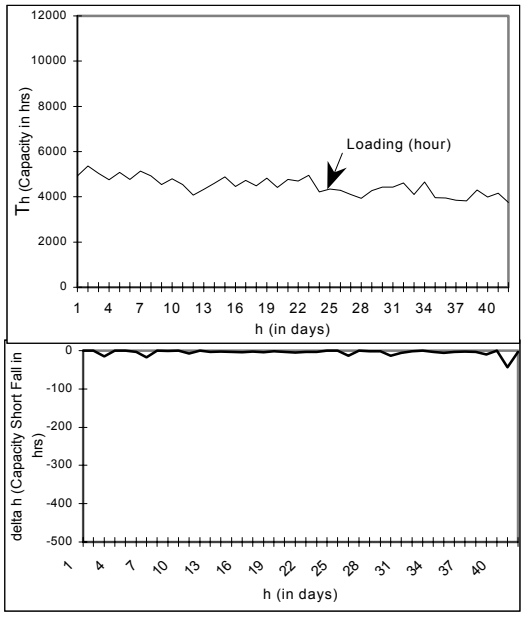

Figure 11: Machine Hours for Rescheduled Lot Release

Table 6 shows the start volumes scheduled over the 42 days period in both experiments together with base data.

Table 6: Start Volume in Lot Release Control Experiments

Total base loading for 42 days	29,222,373
Total loading uniform schedule to machine capacity (series 1)	23,662,985 (19 % below base)
Total loading uniform schedule to 20 % over capacity (series 2)	27,183,929 (7 % below base)

In the new lot release schedule that matched machine capacity, there were 3,090 out of the 15,078 lots that did not have the capacity and therefore were not scheduled. This account for the 19% of the original start volume for the 42

days. In the second series of runs where we created a lot release schedule at a 20 % over-load on the machine capacity hours, the load volume was 7 % lower than the base case.

Table 7 shows the results of the series of runs with lot release control. Here again the respective value of base case is 100 as shown in the first row and the values in parenthesis are actual values in hours for cycle time measures and millions of pieces for throughput.

Table 7: Effect of Smooth Daily Lot Release Scheduling

Change	Max CT Hrs	Mean CT Hrs	98%-ile CT Hrs	Thruput
Base	100 (390h)	100 (141 h)	100 (343 h)	100 (5.54m)
Uniform schedule to capacity- run 1	50 (196 h)	36.1 (51 h)	36.4 (125 h)	96.5 (5.34m)
Uniform - 20% over capacity-run2	54.9 (214 h)	41.1 (58 h)	41.4 (142 h)	109.2 (6.04m)

As shown in Table 7, when uniform lot start schedule is used in the simulation runs, the 98 %-ile cycle time showed a significant reduction of 63% to 125 hours. Here the theoretical ratio of 98 %-ile cycle time is 3.95, based on average theoretical cycle time of 31.6 hours (Table 1). Mean cycle time also showed a significant reduction from 141 hours to 51 hours. Maximum cycle time is halved to196 hours. Despite the 19 % reduction in the start volumes the throughput has only reduced by 3.5 %, indicating a significant reduction in the WIP level. Figure 12 graphically shows the results of the lot release control.

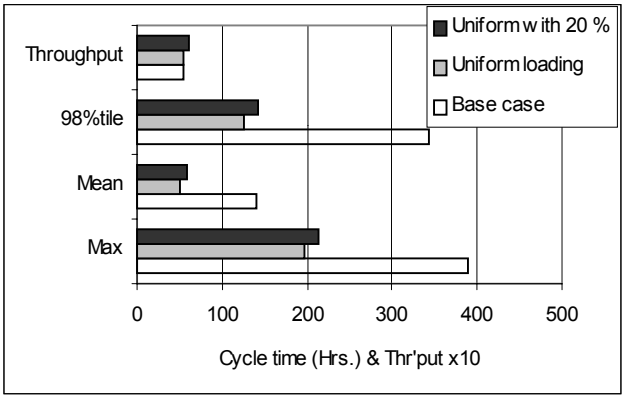

Figure 12: Lot Release Control Results Comparison

In the simulation runs with a uniform release schedule with 20 % over capacity, the 98 %-ile cycle time showed a reduction of 59% from the base case. The 17 hours difference in 98 %-ile cycle time is the cycle time cost of over-loading of starts by 20 % above machine capacity. The new schedule resulted in 7 % less starts than the base but the throughput has increased by 9% from base. Here the theoretical ratio of 98 %-ile cycle time is 4.5. Analysis of the cycle time elements in both series of runs showed that almost the entire reduction is due to queuing time.

These two series of runs confirmed that the erratic schedule is one of the main causes of the excessive cycle time distribution, long no-value-added queue time and failure to achieve the potential throughput. Best cycle time performance is achieved by uniform lot start loading whilst erratic loading results in very long 98 %-ile. In addition loading the lot starts closer to capacity gives the best performance in terms of 98 %-ile at the expense of throughput. Loading above the available capacity has the attraction of minor increases in throughput and machine utilization at the expense of cycle time spread. Loading to capacity results in probably the lowest 98 %-ile but total potential throughput capacity may not be realized. This is mainly due to the fact that no static capacity calculation can predict the exact available hours of every machine family. A leveled loading pattern with slight over-load above the capacity would enable lots to utilize the 'opportunity time slots' arising from the shop floor dynamics and this is a potential area of further research.

The lot release controls used in these simulation runs were based on static calculations of past data. In actual semiconductor manufacturing, static capacity based lot release scheduling is unlikely to give good results as the manufacturing environment is highly dynamic, complex and has alternative routes machine reconfigurations and multitude of physical constraints. A simulation based dynamic lot release scheduling based on multiple criteria and near real time data from the machines and lots would probably be one of the alternatives. Researchers including Sivakumar 1999 have reported simulation based on line near real time lot scheduling in semiconductor backend.

7 CONCLUSIONS

We have presented a simulation-based cause and effect analysis of cycle time distribution in semiconductor backend. We showed how a validated model of an actual semiconductor backend facility was used for the analysis.

The work showed that theoretical cycle time is an important variable that affects the cycle time distribution. In addition each semiconductor factory has different lot sizes for different products based on dice per wafer and other factors and this results in a lot size distribution. Theoretical cycle time distribution and lot size distribution have complex effects on cycle time distribution and further work is required to analyze the cause and effect of these two factors. We have shown that a good operating region for the lot size is between 1500 and 2300 for the semiconductor backend factory for which the analysis was made.

The influence on cycle time spread of factors such as internal material handling, PM, machine failure, and setup are relatively small compare to some other factors in the semiconductor backend factory.

In a limited analysis we have shown that heuristic scheduling policies have some effect on the cycle time spread and no single policy on its own gives the best performance. In general however, ESD heuristics showed the narrowest cycle time distribution.

One of the most significant conclusions from the analysis is that it showed lot release scheduling to the first operation has the greatest impact on cycle time distribution and throughput in semiconductor backend manufacturing. A smooth lot release scheduling in terms of demanded capacity gives short queue time and a cycle time distribution that is significantly narrower than that of an erratic lot release scheduling. Lot release scheduling above the capacity constraint does not improve throughput but substantially add to the cycle time spread.

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