Proceedings of the 2002 Winter Simulation Conference
E. Yücesan, C.-H. Chen, J. L. Snowdon, and J. M. Charnes, eds.

REALIZING 300MM FAB PRODUCTIVITY IMPROVEMENTS THROUGH INTEGRATED METROLOGY

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ABSTRACT

The operational cost of 300mm wafer production is significantly greater than that of 200mm fabs. Real-time monitoring of product can save time and money through reduced scrap and decreased cycle time. Current process monitoring generally incorporates stand-alone metrology, which is time consuming and requires excessive wafer handling by production operators. The benefits of integrated metrology are measured by considering the impact of metrology on a semi-conductor fab through Simulation Modeling. Since the process and metrology steps are in series, overall process throughput depends on metrology methods. Furthermore, the measurements impact WIP (Work In Process) inventory. WIP is at risk if the process drifts. Send-ahead samples reduce WIP risk but also reduce process throughput and tool utilization. Integrated metrology minimizes risk but may decrease throughput rate. This paper explores the operational benefits of integrated metrology strategies versus stand-alone metrology via Simulation Modeling.

1 INTRODUCTION

Though Integrated Metrology is considered beneficial by IC Manufacturers, it is not cost effective to retrofit existing 200mm wafer factories. The strategy then is to explore such issues for 300mm wafer production facilities, and attempt to quantify the benefits of such strategy.

The expected benefits are operational, measured in improved product cycle time, less rework in Lithography, elimination of send-ahead wafers, and a reduction in the number of moves per lot requiring the automated material handling system.

The expected benefits can also be more tactical (or even strategic) in the form of faster time to market due to shorter product cycle time. Integrated metrology can enable Advanced Process Control which in turn can lead to higher wafer yield and better tool performance.

The functional areas of lithography and CMP are explored for the benefits of metrology integration and cost benefit results.

Simulation tools are used to analyze the factory logistics through software products from Brooks Automation Planning & Logistics Division, including AutoSched AP and AutoMod.

When reviewing the literature about the subject of Integrated Metrology (IM), there seems to be two main views: one supporting the use of IM, because it will allow the wafer fab to monitor more closely its functional processing and realize overall fab cost savings (Braun 2002; Collins 2000; Dance, et al, 1998; Haavind 2002; Levy 2001; Spanos 2001). The second is an opposing view that IM is not quite yet up to standards, thus any missed defects will offset any possible gains from lower cost IM modules (Stanley and Maia 2001).

This study attempts to show arguments in favor of the first view, without addressing the second view. The performance of metrology tools or modules is not the authors' area of expertise. However, through simulation studies the authors bring evidence of how IM can perform within a semiconductor fab. It is, therefore, assumed that the integrated metrology module does not significantly differ from a stand-alone metrology tool in its defect identification capability.

The 180nm Aluminum SEMATECH flow was used to provide a basis for discussion with member companies and third parties such as suppliers or OEMs. The general modeling assumptions follow the public International Sematech 300mm factory layout document (Campell, Ammenheuser 2000), modified by the International Sematech 300mm factory modeling presentation (Stanley, et al, 2001). The models simulate a fab with low product mix of 20500 wafer starts per month. The automated material handling system is composed of one inter-bay system and twenty-four intra-bay systems, linked through stockers.

The current industry push towards e-manufacturing and e-diagnostics also brings to the forefront the issue of IM as an enabler for some aspects of these technologies.

2 INTEGRATED METROLOGY ASSUMPTIONS

The role of integrated metrology is not to replace stand-alone metrology tools. However, it will reduce the number of tools needed. Their function will be more out of flow, for calibration, tool matching and backup. This view is supported by (Markle and Arnold 2001).

The functional process areas of lithography and diffusion are explored for the benefits of systematic metrology integration and cost benefit results.

In the lithography functional area it is assumed that an integrated scatterometry module:

- is integrated in the stepper/track system
- measures wafers while other wafers of the same lot are being coated, exposed, baked or developed,
- does not differ significantly from a stand-alone metrology tool in its defect identification capability,
- is capable of CD and Overlay measurements and macro defect identification,
- lengthens the lot processing time at the litho/track system by one minute,
- is complemented with stand-alone metrology tools for CD and Overlay that retake measurements in approximately 20% of the lots processed,
- adds an extra 3 sqft to the footprint of the host tool,
- adds an extra $250K to the purchase cost of the host tool.

In the CMP functional area, and only at front end of the line, it is assumed that an integrated ellipsometry module:

- is integrated in the CMP system,
- measures one wafer while the remaining wafers wait for possible tweak in tool settings,
- does not differ significantly from a stand-alone metrology tool in its defect identification capability,
- is capable of film thickness measurements and can identify dishing and other planarity defects,
- is complemented with stand-alone metrology tools for approximately 20% of the lots processed that retake measurements of film thickness,
- Adds an extra $100K to the purchase cost of the host tool.

3 SIMULATION MODELING AND ANALYSIS

For semiconductor wafer factories, simulation is a very important tool because it allows for an integrated planning, scheduling and dispatching environment that has not been readily available through other modeling tools. Accordingly there is an ongoing International SEMATECH project (started in May 1998) with the objective of using discrete-event simulation modeling to develop an understanding of factory operational issues associated with 300 mm factories. One of these issues is IM (Integrated Metrology) which is much more important in 300mm wafer manufacturing than in 200mm because of the ergonomic requirement leading to a fully automated fab and due to the complexity of 300mm MES software in conjunction with a fully automated material handling system.

The main objective of performing a simulation analysis is to validate the cost analysis conclusions, as well as refine them as appropriate. There are also other types of metrics that can only be obtained through simulation models. For example: Lot Cycle Time average per part type, Average WIP per part type, Queue Time per tool type, Average Transportation Time per lot, Average Time Waiting for Transportation per lot, and Average Number of Moves per lot and part type.

The simulation tools used to analyze the factory logistics are software products from Brooks Automation Planning & Logistics Division, including AutoSched AP and AutoMod. The run time for the models range from 5 minutes per day of simulation, when using the modeled AMHS to calculate transportation times, to 0.5 minutes per day of simulation when using statistics of transportation times collected through simulation or from a fab to emulate the AMHS.

3.1 Base Model Characteristics and Metrics

The base model has been referred in the introduction. The AMHS (Automated Material Handling System) is fully automated. That is, all tools are connected to the AMHS, thus no human intervention is required to move lots, or to load and unload the FOUPs from the tools.

Send Ahead Wafers are modeled as follows: at each litho step, 5% of the lots of each product type go through a "send ahead" route. Lots that are chosen for the Send Ahead route have one wafer split off from the main (parent) lot. This "child" wafer goes through the lithography tool, then through the subsequent metrology steps. After this, the "parent" lot goes through the lithography and metrology steps of the main route. After completing the metrology, the parent and child lots are rejoined.

Also, at each photo layer, 1% to 10% of the lots (depending on the "criticality" of the layer) go through a rework route. No yield loss is assumed.

At each CMP step, a wafer is split off from the lot. The child wafer is polished, then is measured for planarity and thickness. After completing the metrology steps, the remainder of the lot is processed and measured. The parent lot and the child are then rejoined and continue together to the next processing step.

The number of vehicles in the inter-bay AMHS is 35. The number of vehicles in each bay varies between 1 and 3. The layout of the fab in the base model is such that me-

trology tools have been dispersed through the functional areas that require them, so that while the metrology is stand-alone, it is integrated through AMHS in the layout. To accommodate this level of activity and achieve a steady-state factory in a simulation model, the factory equipment census is defined in Table 1.

Table 1: Baseline Equipment Count Results

Functional Area	Tool Count
Lithography	44
CMP	18
Test	17
Implant	6
CVD (non-Metal Dep)	15
Metal Deposition	27
Etch and Strip FEOL	23
Etch and Strip BEOL	32
Thermal (Furnace and RTP)	42
Wet Area FEOL	7
Wet Area BEOL	9
Metrology (Overlay, CD, PLY)	39
Metrology (Film, Visual Inspect)	12

The total tool count of 291 does not reflect any actual factory, but will be used to draw conclusions from the relative usage under different assumptions. This tool count also reflects the modeling design that the Lithography tools are the bottleneck tools of the fab.

In terms of metrics the base model can be described by the following outputs:

- **PW WIP** The average work in process of product wafers (PW), measured by the number of lots of 25 wafers.
- **PW Cycle** Cycle time in days for product wafers.
- **PW X-Cycle** Ratio of cycle time to process time for product wafers.
- **Tr%** Percent of time that a front open unified pod (FOUP) containing a lot is in transport mode.
- **WTr%** Percent of time that a front open unified pod (FOUP) containing a lot is waiting for transport.
- **Tool #** Number of tools defined in the model.
- **Litho times** Queue and processing time at the lithography functional area
- **Litho Metr.** Queue and processing time at the metrology tools associated with the lithography functional area
- **Moves/lot** Average number of moves per lot
- **Rework %** Percentage of lots that must be reprocessed through the same step.

The base model output values are presented in Table 2.

Table 2: Baseline Simulation Results

Metric Description (↓)	Model →	Base
Average WIP (25w/lot)	WIP	626
Ratio of PW Cycle Time to Process time	PW X-Cycle	2.2
Product Cycle Time (days)	PW Cycle	21.3
Transportation Time %	Tr%	<1%
Waiting time for transport %	WTr%	<1%
Tool count	Tool #	291
Litho Area Cycle Time (queue&processing) (days)	Litho CT (d)	7.7
Overlay, CD, & Inspect (queue&processing) (days)	Litho Metrology (d)	2.3
Average number of moves per lot	Moves/lot	983
Rework % in Photo	Rework%	6.4

Three scenarios are considered in comparison to a base case scenario:

1. All the lithography tools have integrated metrology modules installed, but 20% of the regular product flow is also measured at stand-alone metrology tools. The integrated metrology module is also assumed to degrade the throughput of the lithography tool by 1minute per lot of 25 wafers. Send-Ahead wafers are eliminated. Lithography rework percentage is reduced by 17%.
2. The CMP tools have integrated metrology modules installed, but 20% of the regular product flow is also measured at stand-alone film thickness and planarity measurement tools.
3. Both scenarios 1 and 2 have been implemented in the wafer production factory.

The functional areas of lithography and CMP are explored for the benefits of systematic metrology integration and logistics impact.

3.2 Integrated Metrology at the Litho Functional Area

All the lithography tools have integrated metrology modules installed, but 20% of the regular product flow is also measured at stand-alone metrology tools. The Lithography modules of the original flow, as seen in Table 3 below, were modified to obtain an integrated metrology flow. This is shown in Table 4 where 20% of the product lots get extra measurements at the stand-alone metrology tools and the remainder of the lots (80%) use only the integrated metrology in the litho tools:

Table 3: Base Model Litho Processing Times for Non-Integrated Litho Simulations

Process	**Station Family**	**Proc. (min/25 wafer lot)**
Expose Critical	Litho_248	65 mins/lot
Expose Non-Crit	Litho_Iw	55 mins/lot
Meas_CD	Meas_CD_F	16 mins/lot
Meas_Overlay	Meas_Overlay	16 mins/lot
Inspect_PLY	Inspect_PLY	8 mins/lot

Table 4: Litho Processing Times for Integrated Metrology Lithography Simulations

Process	**Station Family**	**Proc Time for 20% of lots**	**Proc time for remaining 80% of lots**
Expose Critcal	Litho_248	66 mins/lot	66 mins/lot
Expose Non-Critical	Litho_Iw	56 mins/lot	56 mins/lot
Meas_CD	Meas_CD_F	16 mins	0 mins
Meas_Overlay	Meas_Overlay	16 mins	0 mins
Inspect_PLY	Inspect_PLY	8 mins	0 mins

The send-ahead wafers in lithography are eliminated through the use of integrated metrology modules installed on the lithography tools. The integrated metrology module is assumed to degrade the throughput of the lithography tool by 1minute per lot of 25 wafers. Also, the rework rate is assumed to be reduced by 1% at each layer, across product types.

The results are compared to the base scenario as seen in Table 5.

Table 5: Integrated Litho Metrology Simulation Results

Model →	**Base**	**Litho IM**
WIP	626	575
PW X-Cycle	2.2	2.1
PW Cycle	21.3	19.6
Tr%	<1%	<1%
WTr%	<1%	<1%
Tool Count	291	291
Litho CT (days)	7.7	2.9
Litho Met CT (days)	2.3	.9
CMP CT (d)	2.7	3
CMP Met CT (d)	.9	.9
Moves/lot	983	837
Photo Rework%	8	5
Litho Idle%	5-11%	10-18%

The CMP processing area cycle time increases slightly. This is due to the fact that the lithography tools can feed the CMP area faster, thus WIP now builds up in the CMP area and must wait longer to be processed.

In comparing the two models in Table 5, the Lithography Integrated Metrology model has 8% less WIP, the cycle time is 8% shorter, and the number of moves requiring the automated material handling system is reduced by 15%. This is due to the effects of WIP being able to move more quickly through the Photo area, which translates to more lots processed per tool per day through a highly reentrant area.

Further experiments show that eliminating the send ahead wafers is responsible for most of the impact shown in Table 5. The cycle time savings without considering send ahead wafers at the Lithography processing and metrology tools are illustrated in Figure 1.

The Lithography functional processing area is by design the bottleneck of the fab in the Base model, thus should realize the most benefits. A previous study (Dance, et al, 1998) showed that the potential benefit of integrating metrology on bottleneck tools is greater than for non-bottleneck tools. One result of integrating the metrology module into the Lithography processing tool, and thus eliminating the send ahead wafers, was that Lithography is not the bottleneck processing area in the Lithography Integrated Metrology Model. It should be noted, however, that this outcome is model specific, and is highly dependent on the usage level in the base model.

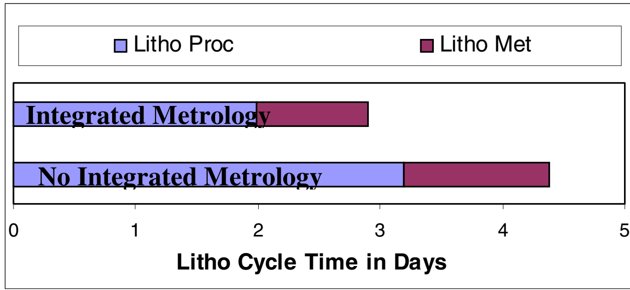

Figure 1: Comparison of Lithography Cycle Time

3.3 Add CMP Integrated Metrology

All the process tools that are followed by a film thickness measurement are considered eligible for integrated metrology, including furnaces, CMP and CVD insulator. The CMP tools have integrated metrology modules installed, but 20% of the regular product flow is also measured at stand-alone metrology tools. It is assumed that there is no impact on throughput.

Processing times in the original flow, as seen in Table 6, were modified to obtain an integrated metrology flow. The second column shows the use of stand-alone metrology, used for 20% of the fab activity. The integrated metrology flow impacting the remaining 80% of the lots processed in CMP is shown in the third column.

Table 6: Processing Time Comparison for CMP Thickness Measurement Simulations

Process	Process time for 20% of lots (min/25 wafer lot)	Process time for remaining 80% of lots (min/25 wafer lot)
CMP Oxide	44	44
CMP Metal & FEOL	40	40
Opti Probe	8	0
Inspect	8	0

The model outputs derived from integrating the metrology in both the Lithography and CMP processing areas can be compared to the Base scenario and with integrating only the Lithography Metrology, as shown in Table 7.

The metrics resulting when both the CMP and lithography metrology is integrated into the host tools improve over integrating only the lithography metrology. The WIP levels decrease by 20% from the Base Model. The product cycle time is almost four days less. The moves required by Automated Material Handling System decreases by a further 15% over integrating the lithography metrology only. The average time that a lot spends in the CMP processing area is one-third that of the Base Model.

Table 7: Results for Integrated Litho and CMP Measurement Simulations

Model →	**Base**	**Litho IM**	**Litho & CMP IM**
WIP	626	575	506
PW X-Cycle	2.2	2.1	1.9
PW Cycle	21.3	19.6	17.2
Tr%	<1%	<1%	<1%
WTr%	<1%	<1%	<1%
Tool Count	291	291	291
Litho CT (d)	7.7	2.9	2.9
Litho Met CT (d)	2.3	.9	.8
CMP CT (d)	2.7	3	.9
CMP Met CT (d)	.9	.9	.3
Moves/lot	983	837	715

3.4 CMP Integrated Metrology

Integrating only the Lithography metrology was considered in Section 3.2. Integrating both Litho and the CMP metrology was considered in Section 3.3. If only the CMP metrology is integrated, while still utilizing the stand-alone CMP tools 20% of the time, the outcome is less dramatic than when only the Litho metrology is integrated, as can be seen in Table 8.

While there is an improvement in the metrics as compared to the Base Model, it is less dramatic than that realized when both Lithography and CMP metrology is integrated as well as when only the Lithography metrology is integrated. This is due to the fact that Lithography is the primary factory bottleneck. Also, most of the CMP steps occur at the end of the product routing flows while Lithography steps occur throughout the flows.

The slight improvement in Cycle Time in the Litho functional area over the Base Model is due to the fact that less inventory is being held up in the CMP area. Thus, lots are able to get to the Litho area faster. The reason for the slight improvement in Litho Metrology cycle time over the Base Model is that some CMP steps share inspection tools with the Lithography area. Less CMP inventory at those inspection tools means that there is more tool availability for the Lithography lots.

4 VALUE OF CYCLE TIME REDUCTION

The advantages of a shorter cycle time have always been of interest to the semiconductor industry. Some of these have

Table 8. Results Comparing CMP Integrated Metrology

Model →	**Base**	**Litho IM**	**Litho & CMP IM**	**CMP IM**
WIP	626	575	506	587
PW X-Cycle	2.2	2.1	1.9	2.1
PW Cycle	21.3	19.6	17.2	20.0
Tr%	<1%	<1%	<1%	<1%
WTr%	<1%	<1%	<1%	<1%
Tool Count	291	291	291	291
Litho CT (d)	7.7	2.9	2.9	7.5
Litho Met CT (d)	2.3	.9	.8	2.2
CMP CT (d)	2.7	3	.9	.9
CMP Met CT (d)	.9	.9	.3	.3
Moves/lot	983	837	715	858

been enumerated by International Sematech (Stanley, et al, 2001). These benefits include:

- Faster yield learning, qualification, and ramp up
- Product in market sooner while sales prices higher
- Faster response to customers' requirements
- Reduce or eliminate contingency buffer lots
- Deliver from production rather than inventory
- Less Work In Process (WIP)
  - Less "At Risk" Inventory due to market change or late discovered defect
- Reduced inspection and clean overhead
- Greater transient throughput.

The advantage of a shorter cycle time in a falling price environment has also been recently addressed by Leachman. Mr. Leachman worked with Samsung to shorten their average cycle-time from 80 days to 30 days over several years. The sales revenues for the DRAM output of Samsung's Kiheung, Korea fab lines over the period March 1996 - December 2000 were tallied at $21.9 billion. By recalculating the sales revenues assuming fab cycle times had stayed at 80 days, Leachman showed the shorter cycle-time increased DRAM sales revenues by US $954 million, or if non-DRAM production is included, the additional revenue from getting products out faster before the price collapses through a shorter cycle-time is $1.1 billion. Samsung's market share also rose from 18% to 22%because of this shorter cycle-time.

Christensen, in a 2001 article, when referring to Leachman's CSM Program, states that "… extending development an extra day, to get a stepper or process qualified, is like paying $3.44 for every wafer that the factory will make. In addition, if it takes one more day to reach mature die yield, it is like paying $1.35 for every wafer that will be made, or if the cycle time is one day longer, it is like paying $3.04 per wafer".

An International Sematech paper (Stanley, Rust, Maia 2001) argues that a reduction in cycle time can be equated to an increase in output. In this case, and if the same proportions are assumed, a reduction of 20% in cycle time could also be taken as an 8% increase in output at the original cycle-time, which is equivalent to 57.6 million dollars per year (8% of 20000 wafer starts per month @ $3000 per wafer).

5 CONCLUSIONS

The results from the experiments show that the modeling assumptions need to be tied more tightly to the operations of the fab, since the benefits depend on those conditions. The real benefits may be tactical (or even strategic) if additional benefits of shorter cycle time are taken into account, as well as less scrap, tighter process capability, and better tool monitoring.

The material handling impact is clearly beneficial, due to the reduction in the number of moves per lot. Thus implementing an integrated metrology strategy could have a large impact on fab layout. The models did not address the layout issue because an International Sematech report (Quinn and Bass 1999) has addressed this issue to some extent by dispersing the metrology tools throughout the functional areas where they are needed. Further studies will require more detailed fab layout definitions.

Integrated metrology has been compared to stand-alone metrology. The cost implications clearly depend on how much integrated metrology modules increase the price of the tool. It could be almost cost neutral if the IM modules cost about 20% of the stand-alone tool, if other impacts are not addressed.

Benefits such as lower cycle time, enabling advanced process control, or advanced equipment control, depend much on the operations of the fab, and so require that the initial conditions be well defined. As an example, the loss of throughput of the stepper/track system may be enough to force the purchase of another system, resulting in a step jump of the processed wafer cost. This alone would make IM not cost effective. The marginal cost and benefit of IM is very dependent on the base conditions to which it is compared.

Integrated Metrology enables Advanced Process Control to realize the benefits of run-to-run control. This is becoming an industry necessity as IC makers move toward 300mm manufacturing. The cost savings and revenue benefits that can be realized from utilizing run-to-run control are impressive (Stanley, Van Eck, Stanley 2002).

The inclusion of measuring, monitoring, and other control mechanisms in the process is common to many other industries other than semiconductor fabrication, and the cost drivers are present (Collins 2000). The major tool suppliers are generally adopting this new paradigm.

ACKNOWLEDGMENTS

This paper was written based on prior work done by Jose' Maia and Tim Stanley. Also, Kristin Rust and Robert Wright deserve special mention for their help with the development of the Base Simulation Model. Dave Benoit of Motorola provided invaluable insight into the inner workings of integrated metrology, particularly scatterometry, in lithography tools.

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APPENDIX

Metrology: Abbreviation for metrology tools or possibly sensors that take measurements of the wafer or of the process.
Stand-alone: metrology tool placed in the metrology bay of the fab.
in-layout: stand-alone metrology dispersed throughout the factory physically close to the wafer processing tools whose output requires measurement.
in-situ: metrology housed within the processing chamber
in-track: metrology in the tool, but not in the processing chamber

in-port: metrology integrated through the load port
in-amhs: metrology in dedicated AMHS loop
Scatterometer: an instrument used to study the nature of scattered light and determine information about a wafer's surface (for example, film thickness, refractive index, and surface contamination).
Ellipsometer: equipment used to measure the thickness and refractive index of dielectric films.
Critical dimension (CD): the width of a patterned line or the distance between two lines, monitored to maintain device performance consistency; that dimension of a specified geometry that must be within design tolerances. Also see line-width.
Overlay (OVL): the precision with which successive masks can be aligned with previous patterns on a silicon wafer.
Front end-of-line (FEOL): all processes from wafer start through final contact window processing.
FOUP: front opening unified pod

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TIMOTHY STANLEY received a BS in Physics from Brigham Young University, an MS in Economics from South Dakota State University, an MS in Nuclear Engineering from the Air Force Institute of Technology, and a Ph.D. in Electrical Engineering from the University of New Mexico. He retired from the US Air Force in 1991, as a Lt. Col. assigned to work with the start-up of SEMATECH and has been instrumental in driving the semiconductor industry transition to 300mm through the original benefit analysis at SEMATECH and as part of the "Startup Team" for SEMICONDUCTOR300 in Dresden, Germany. He currently manages the Productivity Analysis Program for International SEMATECH, which has projects in Industry Economic Analysis, Simulation of 300mm AMHS options, simulation improvement through joint SRC/SEMATECH program called FORCe, and Capital Productivity Analysis for future technology nodes and wafer sizes. His email address is <tim.Stanley@sematech.org>.

JOSÉ MAIA is a professor teaching Industrial Engineering at the Engineering School (IST) of the Technical University of Lisbon. While on sabbatical leave he participated in factory analysis projects at International SEMATECH in Austin/Texas. His working areas include Factory Modeling (automobile industry, paper mill, naval shipyard repair and maintenance), and Systems optimization (oil industry). He received his Civil Engineering, and MS of Operations Research / Systems Engineering from Technical University of Lisbon and his Ph.D. in Management Science from the University of Texas at Austin.