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# USING SIMULATION TO UNDERSTAND CAPACITY CONSTRAINTS AND IMPROVE EFFICIENCY ON PROCESS TOOLS

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## ABSTRACT

Finding hidden capacity and maximizing cluster tool throughput is a common goal for today's semiconductor manufacturers. This presentation will discuss a flexible and accurate simulation program capable of modeling a wide range of semiconductor process tools. The simulation program provides visibility and understanding into the internal dependencies and interactions of each process tool. This information provides a solid base from which sound decisions can be made. Simulation results from two case studies will be presented. The real-world capacity improvements, cycle time reductions and cost savings will be presented.

## 1 INTRODUCTION

Texas Instruments Incorporated (TI) is the world leader in digital signal processing and analog technologies, the semiconductor engines of the Internet age. DMOS5 is one of TI's wafer fabs that currently manufactures many products for the analog/DSP business of TI, making it a high volume/high mix wafer fab.

Simulation has been used as a marketing, engineering, and scheduling tool for years in the semiconductor industry with varying degrees of success. Simulation case studies have analyzed factors such as wafer-handling options, process tool configurations, processing times, lot sequencing, batch sizes, wafer metrology schedules, and other activities and have evaluated their effects on throughput. Sometimes, simulation results have motivated changes in original tool designs, resulting in alternate configurations that provide better throughput performance at less cost. More common, however, simulation results provide information that can be used by equipment owners to optimize the tools performance.

The application of simulation software to real-world semiconductor equipment faces several challenges. For a simulation effort to have a greater chance of success, the software must be fast, easy to use, flexible, and accurate. Since conditions in a fab change daily, the time required to adapt the simulation model to the current conditions must also be fast. In addition, the variety and complexity of semiconductor equipment requires flexibility in the software. Finally, for a simulation model to be of any worth it must accurately represent the tool.

The ToolSim software was chosen for this case study. ToolSim is a growing library of flexible simulation models developed using the AutoMod™ simulation software. ToolSim is capable of quickly and accurately modeling a wide range of semiconductor process tools, including PVD, CVD, Etch, Photolithography, and CMP equipment.

## 2 CLUSTER TOOLS

The focus tools in this study are specific deposition (CVD) cluster tools. A cluster tool is an integrated, environmentally isolated, wafer manufacturing system consisting of processing chambers, internal robots to transport wafers, and load locks where the wafer-to-cassette exchange takes place. The primary function of a cluster tool is wafer processing. Wafers enter the cluster tool inside a carrier, commonly called a cassette or FOUP. Each wafer undergoes a number of sequential process steps before leaving

the tool. Each step in the wafers routing moves the wafer to the respective processing chamber where material is deposited on the wafer or the wafer is enhanced in some way. Wafers are transferred from tool to tool in atmosphere. Atmospheric exposure can be destructive to the wafer film, reducing product yields. Cluster tools provide a means of grouping a number of evacuated, isolated processing chambers together in an evacuated area. This evacuated cluster improves the "clean room' environment and reduces the number of atmospheric moves required by the wafers. In turn, product yields are improved and cycle times are reduces. Figure 1 illustrates the base components in a typical cluster tool.

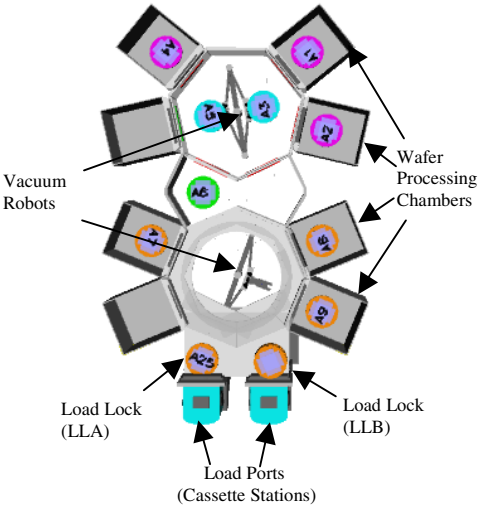


Figure 1: Typical Cluster Tool

Semiconductor manufacturing equipment (cluster tools) continues to increase in complexity. Throughput rates, cycle times, and chamber utilization's can not be calculated based on processing times alone. System parameters such as wafer sequencing, robot speeds, pump and vent times, clean cycles and other parameters can create system dependencies that effect throughput. Because of the many possible tool configurations and wafer routing combinations, simulation has become a necessity in predicting and optimizing cluster tool performance.

## 3 FLEXIBLE SIMULATION MODEL

Cluster tools encompass a wide range of configurations and wafer flows. Therefore, the ToolSim simulation model, developed by Brooks Automation, was built as a flexible, data-driven template model.

Data sets are used to configure and drive the simulation model. A data set consists of many different input files. These data files define the tool configuration and other model options used in the simulation run. Data input includes items such as the number and location of processing chambers and load locks, chamber-processing times, wafer route sequence, pump and vent times, number of slots in the load locks and many others. All of the relative operational parameters of the real-world system are defined through data input. The simulation model reads the data set at the beginning of the simulation run, configures the model both graphically and statistically, and provides the corresponding output. The flexibility of the simulation model includes the ability to configure it to run under any real-world tool configuration.

## 4 CASE 1: CHAMBER CLEANING EFFECTS

Using the ToolSim "cluster" module, the Texas Instrument Industrial Engineering quality improvement team (QIT) was able to model a three chambered deposition tool and determine the impact of changing clean cycles. The wafer sequence (route) on this tool consists of three steps:

Step 1: Processing in 1 of 3 deposition chambers
Step 2: Processing in an 8 Slot cool chamber
Step 3: Returning to the 25 Slot Load Lock

This deposition cluster tool is graphically illustrated in Figure 2.

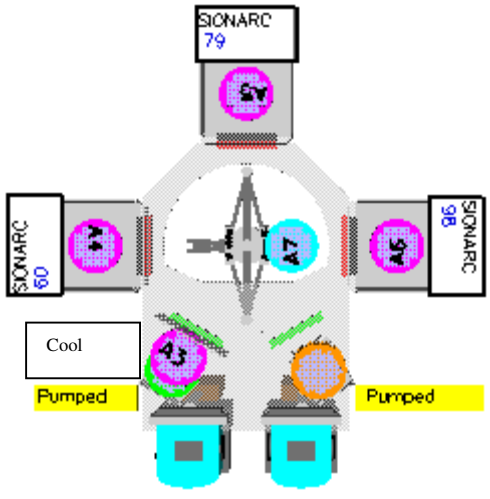


Figure 2: Case 1 Deposition Cluster Tool Illustration

### 4.1 Clean Cycles

Processing chambers often need to go through a self-cleaning cycle to purge chamber impurities that may build up during processing. Clean cycles are typically triggered after the chamber has processed a certain number of wafers. The clean cycle begins once the trigger wafer is removed from the chamber. The chamber will not process another wafer until the clean cycle is finished.

Case 1 processing chambers were cleaned after processing every 8 wafers. The Process Engineers determined that changing the cleaning frequency to clean after processing every 16 wafers would have little effect on yield. The simulation model was used to quantify the throughput changes as a result of changing clean frequencies.

### 4.2 Case 1 Scenario Runs

Simulation scenarios were set up and run to understand the effect that changing clean cycle frequency has on throughput. Table 1 contains the simulation results for the case 1 scenario.

Table 1: Case 1 Simulation Results

| Clean Frequency | Throughput (Wafers per Hour) |
|---|---|
| 8 | 17.7 |
| 9 | 17.7 |
| 10 | 18.7 |
| 11 | 18.7 |
| 12 | 19.9 |
| 13 | 19.9 |
| 14 | 21.4 |
| 15 | 21.4 |
| 16 | 21.8 |
| 17 | 21.8 |
| 18 | 22.4 |
| 19 | 22.4 |
| 20 | 22.8 |

The graph of the simulation results, along with the estimated yield loss related to the cleaning cycles are illustrated in Figure 3.

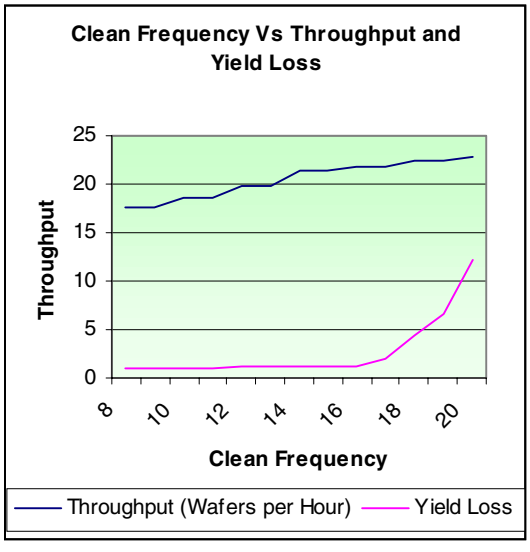


Figure 3: Case 1 Simulation Results

### 4.3 Case 1 Simulation Results

The simulation model was validated against the current operational parameters of the cluster tool, providing confidence the simulation model was accurate. Simulation throughput predictions consistently fell within 2% of the real-world base tool. The simulation scenario was then set up and run to provided throughput results for the clean frequency range, before any changes were made in the fab. Changing the cleaning frequency from every 8 wafers to every 16 wafers increased the tool throughput rate from 17.7 WPH to 21.8 WPH, and increase of 23%. In addition, since the cleaning cycles now occur less frequently, the cleaning chemical savings resulted in $38,000 a month per tool.

The simulation effort provided visibility and credibility to the proposed solution, and facilitated a faster decision by upper management to implement the recommended change.

## 5 CASE 2: CHAMBER REQUIREMENT STUDY

Using the ToolSim "dual cluster" module, the Industrial Engineering Quality Improvement Team was able to model a dual-clustered multi-chambered sputter tool and determine the impact of changing configurations. This tool processed multiple products. Both products complete similar process steps, but use different processing times in the "TI" or "DLXTIN" chambers. Figure 4 illustrates the tool configuration with two "TI" and two "DLXTiN" chambers.

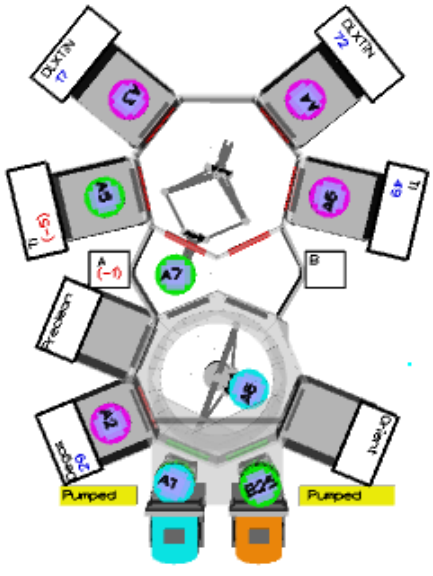


Figure 4: Dual Cluster Sputter Tool Configuration

### 5.1 Sputter Tool Configurations

Cluster tools can be configured to many different configurations. Processing chambers can be attached and used at the tool facet locations. It is not necessary for processing chambers to be attached at all facets of the tool. There is a cost associated with attaching and maintaining processing chambers that are not needed. There are also costs associated with having too few processing chambers. Therefore, depending on the processing requirements, there is an optimal configuration for each tool. Simulation was used to determine the optimal configuration.

Three configurations were simulated. Table 2 contains the parameters for these three configurations

Table 2: Sputter Tool Configurations

| Configuration | Number of TI Chambers | Number of DLXTiN Chambers |
|---|---|---|
| Initial | 1 | 1 |
| Configuration 1 | 1 | 2 |
| Configuration 2 | 2 | 2 |

### 5.2 Case 2 Scenario Results

Simulation scenarios were set up and run to understand the effect that tool configuration has on throughput. The simulation model was validated against the Initial tool configuration, providing confidence the simulation model was accurate. The simulation results are summarized in table 3.

Table 3: Simulation Results

| Configuration | Maximum Throughput Achieved (WPH) |
|---|---|
| Initial | 30.9 |
| Configuration 1 | 41.3 |
| Configuration 2 | 42.2 |

The throughput calculations were based on the assumption that the tool is being fed continuously, that the tool is processing product in a serial mode, and that there are no chamber cleaning cycles.

The simulation results show that configuration 2 will improve throughput on the current tool by 34%. There is only a small throughput improvement of 2% when you move from Configuration 2 to Configuration 3 (adding a second TI chamber).

From the simulation output, the optimal configuration proved to be configuration 2, which uses 2 DLXTiN chambers and 1 TI chamber. The throughput increase of adding the second TI chamber didn't justify the capital investment. Therefore, a costs savings of $26,000 was realized for each sputter tool in the tool set. In addition, by upgrading the configuration from the initial configuration to configuration 2, each tool in the tool set improved productivity by 34%. This additional throughput more than offset the costs associated with adding the additional DLXTiN chamber.

## 6 CONCLUSIONS

The increasing complexity and versatility of cluster tools and other semiconductor equipment has created a need for simulation to accurately predict tool performance. The integration of variable configurations, robot options, product routes, chamber processing times, clean cycles, and many other tool parameters (which together make up a seemingly infinite number of run possibilities) can easily be evaluated using simulation. The flexible, accurate, and easy to configure program provides the understanding and confidence necessary to optimize cluster tools.

The QIT team at TI was able to analyze and document savings on two case scenarios as summarized in Table 4.

Table 4: Benefit Summary

| Case | Process | Change Assessed | Results | Fab decision affected |
|---|---|---|---|---|
| Case 1 | Sion | Reduction of Cleaning Cycles | Savings of $4M / year. (Two tools gained $6M). | Cleaning Cycle Implemented across the toolset |
| Case 2 | CVD TiN | Addition of DLX Chambers | Improved throughput by 34% by adding second DLXTI chamber. Saved $26K per tool by not adding second TI chamber. | 2 DLX chambers were added to each of the tools in the ToolSet. |

These two case scenarios illustrate a small sample of the types of issues simulation has been used for in the semiconductor equipment industry. Simulation has proven to be an effective analytical tool at Texas Instruments DMOS 5.

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## AUTHOR BIOGRAPHIES

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