

## **APPLICATION OF CLUSTER TOOL MODELING TO A 300 MM FAB SIMULATION**

Sameer T. Shikalgar  
David Fronckowiak

IBM Microelectronics Division  
East Fishkill, NY 12533, U.S.A.

Edward A. MacNair

IBM T.J. Watson Research Center  
Yorktown Heights, NY 10598, U.S.A.

### **ABSTRACT**

300 mm semiconductor wafer fabrication facilities, like conventional semiconductor fabs, contain many different types of tools. In this paper we discuss a realistic way of representing cluster tools in a simulation model of the entire line. A more realistic representation of cluster tools results in greater accuracy in the output of the simulation model.

### **1 INTRODUCTION**

A semiconductor wafer fabrication line is a very complicated system with many tools and products. The products travel through the same tool groups repetitively using reentrant flows. Attempts to model this type of system with a spreadsheet do not capture all of the complexities in a semiconductor line. We have been modeling a 300 mm line for more than six years using simulation models to represent a realistic view of the system (Campbell and Latinen, 1997; Campbell and Norman, 1998; Campbell and Norman, 1999; Campbell, Rohan, and MacNair, 1999; Shikalgar, Fronckowiak, and MacNair, 2002; Norman, and Barksdale, 1999).

Semiconductor lines use tools called cluster tools. Cluster tools contain multiple chambers with one or more robots moving wafers through the chambers. A number of people have studied cluster tools (Dummler, 1999; Govind, and Fronckowiak, 2003; Koehler, Wulf, Bruska, and Sepanen, 1999; LeBaron and Hendrickson, 2000; LeBaron, and Pool, 1994). The 300 mm model, which this paper is based upon, represents the entire fabrication processing of a wafer. It contains hundreds of tools, more than 50 product flows, reticles, operators, tool down times, scheduled preventive maintenance times, and other complexities found in the system. We have incorporated an accurate presentation of cluster tools in the model.

In Section 2 the advantage of modeling cluster tools is discussed. Section 3 describes the model details. In Section 4 the functioning of the model is discussed. The data collection necessary to represent cluster tools is discussed in

Section 5. Section 6 gives the experiments that were conducted using the model. The last two sections describe the results obtained and the run lengths.

### **2 ADVANTAGES OF CLUSTER TOOL MODELING**

The representation of cluster tools in the simulation model requires substantially more data than the original representation, but provides a much more realistic version of processing. Modeling of cluster tools provides the ability to represent each process on a cluster tool with great accuracy. Many cluster tools do not perform similar operations on every chamber. Moreover different chambers may be used during different steps in the route depending on the mask level. Modeling different chamber types on a cluster tool assists in identifying specific bottleneck processes on a cluster tool. The traditional way of modeling cluster tools in a simulation is by modeling the bottleneck chamber on the cluster tool. This can lead to flawed statistics, like average processing time, where the time spent by the wafer in non-bottleneck chambers is not accounted for in serial cluster tools.

### **3 MODEL DETAILS**

The simulation model was built with simulation tools from Brooks Automation, including AutoSched™ AP and AutoMod™. The original simulation models that were built had three types of tools: wafer by wafer, batch, and pipeline. Wafer by wafer tool processing includes the fixed time for the entire lot, as well as time for each wafer. Batch tools accumulate lots into a batch, and process the batch of lots together. Pipeline tools process batches of lots in a sequence of tanks. This is used to model wet benches. The three types of tools described above do not capture the processing complexity at many of the tools in the fab. Brooks Automation provides a semiconductor extension, which more accurately represents chamber tools and wet benches (Brooks Automation, Inc., AutoSimulations Divi-

sion, 2001). It allows the definition of cluster tools, chambers, robots, and cluster tool routes. Cluster tools contain multiple chambers, and the cluster tool routes allow you to specify the order in which the chambers are used. Different products and different steps of the same product can move through the chambers in different orders. Many wet benches have the additional complexity that more than one lot can be batched and processed as a unit through the tools. The standard functioning of the semiconductor extension was changed to accommodate the requirement for batching lots at cluster tools.

Different types of tools are represented as cluster tools in the model, for example, photolithography, plasma etchers, strippers, wet chemical cleans, platers, rapid thermal processing, chemical vapor deposition, and chemical mechanical polishing. Modeling of a wide range of cluster tools necessitated further classification to account for various processing differences. The modeled cluster tools are classified into the following subcategories:

**Parallel Processing Cluster Tools:** These are cluster tools that have one or more chambers on them that perform similar operations. A wafer that is processed on these cluster tools is required to visit only one chamber on the cluster tool. For example, a strip tool can have more than one strip chamber that performs the same operation on a wafer.

**Serial Processing Cluster Tools:** These are cluster tools with more than one chamber type. A wafer is transported from one chamber type to the other using a wafer handler robot. A wafer is required to visit all chamber types on the cluster tool to successfully complete the operation. A photolithography tool is an example of this type of cluster tool. The different stages on the track and the scanner of a photolithography tool are modeled individually as chambers.

**Batch Processing Cluster Tools:** The chambers for these types of cluster tools can combine more than one lot to form a batch. The batch moves through the cluster tool as a single entity until it has finished processing. This is mainly used to model wet benches where each tank in a wet bench is modeled as a chamber.

## **4 MODEL FUNCTIONING**

Cluster tools are defined in the station file of the simulation model. A subroute needs to be defined for each operation that a cluster tool is qualified for. A subroute is a sequence of chamber types within the cluster tool that define the path for processing a wafer. When a lot reaches a step in its route that requires a cluster tool, it is pushed onto a subroute that is defined for the step. The lot is held at the step until all the wafers complete processing through the cluster tool.

## **5 DATA COLLECTION**

The data representing the cluster tools in the model is updated in two separate spreadsheets. The first spreadsheet consists of tool specific information such as tool id, number of chambers, and type of each chamber. The second spreadsheet consists of subroute specific information for each step that the cluster tool is used in the route. Subroute specific information consists of the chamber type used and the processing time for each wafer or batch. Subroutes are defined for each operation for each cluster tool.

Operation and tool specific data can change periodically depending on new processes on a tool, new chambers added to an existing tool or a new cluster tool added to the model. An external program is used to transform the data in the spreadsheet, to a format that is readable by the simulation model.

## **6 EXPERIMENTS**

Different types of experiments were performed with the cluster tool representation that is discussed above. Originally the experiments were used to help make strategic design decisions for the line. This started before the line was built and in production. Experiments have been conducted on the ramp up phase of the fab, as well as the full production environment. The model has also been used to make operational decisions for the daily working of the fab.

Experiments were also conducted to articulate the differences between a cluster tool and a non-cluster tool model. A non-cluster tool model was developed using the same parameters from the cluster tool model except that all chamber and subroute information was removed from the model. Comparisons of fab parameters like average cycle time, average WIP and throughput illustrate significant changes to the representation of the fab. Additionally the effect of each type of cluster tool, defined in Section 3, is summarized to quantify the impact to overall raw process time and cycle time.

## **7 DISCUSSION OF RESULTS**

The two models were run for the same time period with the same number of tools, products and the same wafer start profile. As shown in Figure 1, the non-cluster tool model showed a significant difference in the average WIP in the fab.

Correspondingly the average cycle time for the fab is longer and the average throughput of the fab is lower as shown in Figure 2.

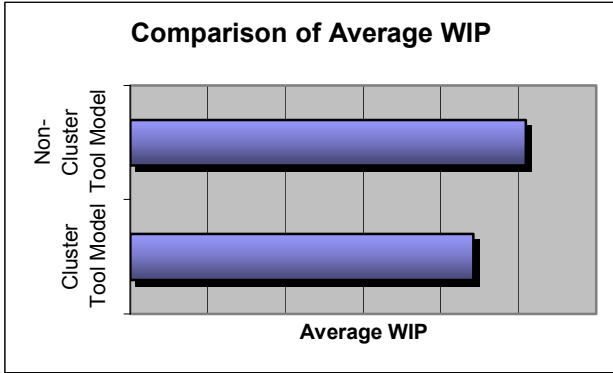


Figure 1: Comparison of Average WIP

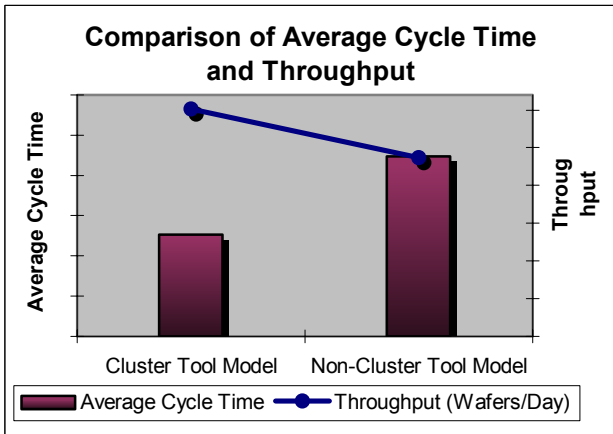


Figure 2: Comparison of Average Cycle Time and Throughput

These differences can be attributed to different processing times on each cluster tool. Depending on the type of cluster tool, the processing time shows a significant difference, as seen in Figure 3.

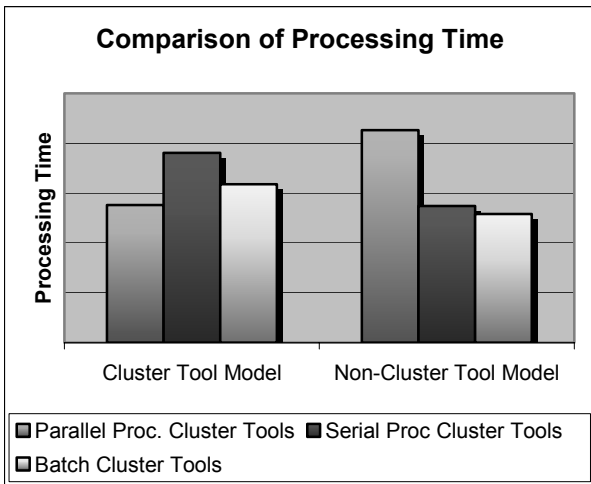


Figure 3: Comparison of Processing Time

Figure 3 shows that the number of modeled cluster tools, of a particular type, influences the processing time of the fab. The processing time for parallel cluster tools is lower in the cluster tool model since the cluster tool model distributes the wafers in a lot to available parallel chambers on a cluster tool. The serial cluster tools have a lower processing time in the non-cluster tool model since the lot processing times in the non-bottleneck chambers is not accounted for. This shows that a non-cluster tool model of a fab would have inaccurate processing times and hence inaccurate cycle times.

## 8 RUN LENGTHS

The run lengths of the model vary with the number of wafer starts per day and with congestion in the model. If the bottleneck tool has more than 10% idle time, a warm-up of 40 days and a steady state phase of 80 days provides sufficient accuracy. If the bottleneck tool has between 5% and 10% idle time, a warm-up run of 100 days and a steady state of 300 days is required. If the bottleneck tool has less than 5% idle time, a very long run may be required to obtain accurate results. Many of the runs take between four and five hours for the cluster tool representation of the model.

The non-cluster tool model, however, runs considerably faster than the cluster tool model. Less data and lower computation required for a non-cluster tool model results in faster run times.

## 9 SUMMARY

The processing that takes place at many of the tools in a 300 mm wafer fabrication line is complicated and not easily captured by a traditional approach. A more realistic representation of modeling cluster tools has been discussed. This representation provides greater accuracy in the results. Also, not modeling cluster tools may lead to misleading results and erroneous conclusions.

## ACKNOWLEDGMENTS

We wish to acknowledge the discussions and contributions from our colleagues including Richard Burda, Jeffrey Gifford, Nirmal Govind, Randy Harris, Stacy Higley, Lauren Karpiszyn, Patrick Kendell, Keila Martinez, John Muscatello, and Chaunese Turner.

## REFERENCES

- Brooks Automation, Inc., AutoSimulations Division. 2001. AutoSched AP Customization Guide v 7.0.
- Campbell, P., and G. Laitinen. 1997. Overhead Intra-bay Automation and Microstocking – a virtual fab case study. In *Proceedings of the IEEE/SEMI Advanced*

*Semiconductor Manufacturing Conference and Workshop*, 368-372. Cambridge, MA.

- Campbell, P., and M. Norman. 1998. Microstocking and Fab Throughput. In *Proceedings of the AutoSimulations '98 Symposium*, 101-106. Bountiful, UT.
- Campbell, P., and M. Norman. 1999. Simulation Used To Model And Test Improvements In 300 Mm Fab Throughput. Available online via <<http://www.semicondutoronline.com>>.
- Campbell, P., D. Rohan, and E. MacNair. 1999. A Model of a 300mm Wafer Fabrication Line. In *Proceedings of the 1999 Winter Simulation Conference*, ed. P.A. Farrington and H.B. Nemhard, 909-911. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers.
- Dummler, M. 1999. Using Simulation and Genetic Algorithms to Improve Cluster Tool Performance. In *Proceedings of the 1999 Winter Simulation Conference*, ed. P.A. Farrington and H.B. Nemhard, 875-879. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers.
- Govind, N., and D. Fonckowiak. 2003. Resident-Entity Based Simulation of Batch Chamber Tools in 300mm Semiconductor Manufacturing. Submitted to *Proceedings of the 2003 Winter Simulation Conference*, ed. S. Chick, P. J. Sánchez, D. Ferrin, and D. J. Morrice.
- Koehler, E., T. Wulf, A. Bruska, and M. Sepanen. 1999. Evaluation of Cluster Tool Throughput for Thin Film Head Production. In *Proceedings of the 1999 Winter Simulation Conference*, ed. P.A. Farrington and H.B. Nemhard, 714-719. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers.
- LeBaron, T., and R. Hendrickson. 2000. Using Emulation to Validate a Cluster Tool Simulation Model. In *Proceedings of the 2000 Winter Simulation Conference*, ed. Jeffrey A. Joines and Russell R. Barton, 1417-1422. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers.
- LeBaron, T., and M. Pool. 1994. The Simulation of Cluster Tools: A New Semiconductor Manufacturing Technology. In *Proceedings of the 1994 Winter Simulation Conference*, ed. Jeffrey D. Tew and S. Manivannan. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers.
- Norman, M., and J. Barksdale. 1999. Integrated Manufacturing and Material Handling Simulation Modeling. In *Proceedings of the SIMULATION Solutions '99 Conference*. Mesa, AZ.
- Shikalgar, S., D. Fronckowiak, and E. MacNair. 2002. 300mm Wafer Fabrication Line Simulation Model. In *Proceedings of the 2002 Winter Simulation Conference*, ed. Enver Yucesan and Chun-Hung Chen, 1365-1368. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers.

## AUTHOR BIOGRAPHIES

**SAMEER T. SHIKALGAR** is an Industrial Engineer in IBM's Microelectronics Division. He has worked in the areas of modeling and analysis of semiconductor processes. He holds a M.S. in Industrial Engineering from Virginia Polytechnic and State University and a B.E. in Production Engineering from Mumbai University, India. His email address is <[sshik@us.ibm.com](mailto:sshik@us.ibm.com)>.

**DAVID FRONCKOWIAK** is the manager of the 300mm Industrial Engineering Department in IBM's Microelectronics Division. He has worked in the modeling and simulation of semiconductor processes with emphasis on fab productivity improvement for 10 years. He holds a M.S. in Industrial Engineering from the University of Arizona and a MBA from Marist College. His email address is <[fronckow@us.ibm.com](mailto:fronckow@us.ibm.com)>.

**EDWARD A. MACNAIR** specializes in modeling contention systems in IBM Research's Mathematical Sciences Department. He has more than 38 years of experience at IBM and has worked in the areas of modeling systems and model tool development. Mr. MacNair holds a M.S. in Operations Research from New York University and a B.A. in Mathematics from Hofstra University. His email address is <[emacnair@us.ibm.com](mailto:emacnair@us.ibm.com)>.