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A FRAMEWORK FOR STANDARD MODULAR SIMULATION IN SEMICONDUCTOR WAFER FABRICATION SYSTEMS

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ABSTRACT

This paper presents the application of a framework, proposed by the National Institute of Standards and Technology (NIST), for standard modular simulation in semiconductor wafer fabrication facilities (*fabs*). The application of the proposed framework resulted in the identification and specification of four different elements in the context of semiconductor fabs: (1) market sector, (2) hierarchical modeling levels, (3) simulation case studies, (4) models and data. An example of the application of the proposed simulation framework to a benchmark semiconductor fab model, the so-called *Mini-fab*, is presented. In this example, evaluation of production performance under different workforces is studied. Current and future research is focused on the improvement of the proposed framework (e.g., design and testing of generic case studies).

1 INTRODUCTION

Simulation models for semiconductor wafer fabrication are considered important tools for supporting the decision-making processes in manufacturing operations. Although the importance of simulation models has been clearly stated (Kelton, Sadowski, and Sturrock 2003, Law and Kelton 2000), currently there is no standardization for models and data or simulation case studies in the semiconductor industry. In general, each commercial simulation software vendor offers its own data formats for modeling and data representation. The non-existence of standards in this area thus increases the difficulties associated with the simulation process when a model of the semiconductor fabrication facility or *fab* does not exist, and simulation case studies need to be designed.

Members in both the industry and academic communities have indicated in the past (Fowler, Fu, Schruben, Brown, Chance, Cunningham, Hilton, Janakiram, Stafford, and Hutchby 1998) the clear need for standardization of modeling data in semiconductor manufacturing. For instance, an attempt for obtaining a standard was presented by SEMATECH with the so-called *Modeling Data Standards* (MDS) (SEMATECH 1997), and another initiative, from Semiconductor Equipment & Materials International (SEMI), was mentioned in (Fowler, Fu, Schruben, Brown, Chance, Cunningham, Hilton, Janakiram, Stafford, and Hutchby 1998); however these attempts have had little or no success at all. According to some experts in this simulation field (Fowler 2004), it appears that these attempts have not been attractive for the commercial vendors of simulation software for commercial reasons.

Although these attempts have failed in the past, the importance for standardization of modeling data is still needed, and this could represent a valuable improvement in current simulation practices. In an attempt to narrow this gap, the National Institute of Standards and Technology (NIST) has identified the need for standards in simulation and modeling in different industries, including the semiconductor manufacturing industry. Work is being conducted by NIST, within the S*ystem Integration of Manufacturing Applications (SIMA)* program, to provide standards in simulation of manufacturing systems that in the future can facilitate the work of simulation groups or analysts at different industries. Part of the efforts has been in the formulation of a *Framework For Standard Modular Simulation* (McLean and Leong 2002, McLean and Shao 2003), and *Standard Exchange Data Formats* (Lee and McLean 2003) that could facilitate the utilization of simulation models and case studies with different commercial simulation packages utilized in the manufacturing industry.

The main objective of this paper is then to present a framework for modular simulation of semiconductor fabs and an example of its application. We propose this framework based on the approach presented in (McLean and Leong 2002, McLean and Shao 2003) and by providing

details of each element in the framework in the context of the semiconductor manufacturing industry.

The following is the organization of this paper: section 2 presents an overview of NIST's SIMA program. In section 3 we present a brief overview of the semiconductor manufacturing process at the fabrication level and how simulation is utilized at this level. The application of the framework for standard modular simulation for semiconductor wafer fabrication is presented in sections 4, 5, and 6, and an example is provided in section 7. Finally, a summary and conclusions are given in section 8.

2 NIST SYSTEM INTEGRATION OF MANUFACTURING APPLICATIONS (SIMA) PROGRAM

The High Performance Computing and Communication (HPCC) program was formally established by the High Performance Computing Act of 1991 (Public Law 102-194). The goal of this program is to accelerate the development of future generations of high performance computers and networks and the use of these resources in the government and throughout the U.S. economy. The SIMA program at NIST is the agency's coordinating focus for its HPCC activities. SIMA is addressing the information interface needs of the U.S. manufacturing community by focusing on defining, testing, and promoting standards for interoperability solutions, and by facilitating remote access to scientific and engineering data.

The Manufacturing Systems Integration Division (MSID) was established to contribute to the research and development of data standards, generic interfaces and technologies leading to the implementation of virtual manufacturing enterprises and supply chain management systems.

MSID has been working on the development of a generic manufacturing information model for representing and exchanging production simulation data. This document presents an information model that provides neutral data interfaces for integrating machine shop software applications with simulation. The model is presented by using the Unified Modeling Language (UML) (Object-Managment-Group 2005) and the eXtensible Markup Language (XML) (World-Wide-Web-Consortium 2005). The initial emphasis of this data model is focusing on the machine job shop definitions. Plans are in place to extend the data structures to include other relevant areas such as supply chain, plant layout, and assembly.

As a part of the standards development effort, NIST has organized a Product Development Group (PDG) titled, *Core Manufacturing Simulation Data* (CMSD) within the Simulation Interoperability Standards Organization (SISO). The model will be the strawman of the first product of the CMSD PDG. SISO is dedicated to the promotion and development of standards for Modeling and Simulation (M&S), system interoperability, and reuse for the benefit of diverse M&S communities, including developers, procurers, and users, in the world-wide simulation communities. For more details see (McLean, Lee, Shao, and Riddick 2005).

MSID has partners in industry end-users, software vendors and government agencies with diverse interests such as: steel fabrication, electromechanical production, semiconductor, die casting, injection molding, machining, automotive and aerospace assembly, inspection, human operator modeling, ergonomics analysis, supply chain, discrete event models, and graphical representations.

3 BRIEF OVERVIEW OF SEMICONDUCTOR MANUFACTURING SYSTEMS

The fabrication of semiconductor devices or integrated circuits (IC), also known as semiconductor manufacturing, involves four basic steps (Uzsoy, Lee, and Martin-Vega 1992, Plummer, Deal, and Griffin 2000): *wafer fabrication*, *wafer probe*, *assembly*, and *final test*. The wafer probe and fabrication are considered as *front-end* processes, which are dedicated to building the ICs in the silicon wafer as well as performing preliminary tests. The assembly and final test are considered as *back-end* processes that are focused on testing functionality and performance, and finally packaging of the ICs. In this paper we are focused on the modeling and simulation of the semiconductor wafer fabrication process that takes place in the semiconductor fab. In general, we refer to the simulation of the semiconductor fab when we talk about simulation of the wafer fabrication process.

Semiconductor wafer fabrication is probably one of the most intensive manufacturing processes, not only for its complexity but for the amount of capital invested. It usually involves several hundreds of processing steps. Moreover, since the number of operations that have to be carried out exceeds the number of available machines, several of these operations are done at the same work centers or *tool stations*. This means that wafer lots visit a tool station more than once. A manufacturing system having this feature is called a *re-entrant line* (Kumar and Kumar 2001). In addition, some wafers could need rework during the production, which makes the process more complicated.

Simulation models are utilized in semiconductor manufacturing at different levels (see Figure 1 (Li, Ramírez-Hernández, Fernandez, McLean, and Leong 2005)). In the case of wafer fabrication (i.e., front-end processes), simulation models are utilized to address different and complex operational problems (e.g., job scheduling, material handling, lots releasing control). This task is performed by defining simulation case studies that are used to answer questions (e.g., "what-if" questions) about specific problems. The conclusions derived from the simulation work can help to improve manufacturing operations by imple-

menting alternative strategies that have been analyzed and validated through a simulation analysis procedure.

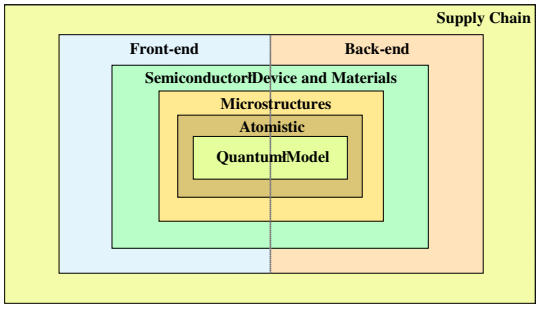

Figure 1: Simulation Hierarchy in Semiconductor Manufacturing

4 FRAMEWORK FOR MODULAR SIMULATION OF SEMICONDUCTOR FABS

In this section we describe a framework for modular simulation of semiconductor fabs, which is based on the general framework presented by McLean & Leong in (McLean and Leong 2002).

The main motivation of the framework presented in (McLean and Leong 2002) was the non-existence of standards for simulation models and data in several industry sectors. A clear example is the current semiconductor industry where there is no standardization in the models and data utilized in the simulation of the fabs. The lack of standards usually increases the amount of work and costs involved in the modeling and simulation process.

The primary objective of the framework proposed by McLean & Leong (McLean and Leong 2002) was to provide a scheme for the identification of the modules and data required to address various types of simulation problems. In addition, they suggested that a standard framework could facilitate the exchange of data, models, and case studies between commercial simulation software, and therefore, accelerate and facilitate the overall simulation process. For instance, the development of standard templates or modules for different types of case studies would be a step to minimize duplication of simulation work, reducing the modeling process and costs. As depicted in Figure 2, the framework proposed in (McLean and Leong 2002) includes the following four general elements or categories: *(1) Market Sector, (2) Hierarchical Modeling Levels, (3) Simulation Case Studies,* and *(4) Models and Data.*

The market sector, hierarchical modeling levels, and simulation case studies layers can be utilized for identification purposes rather than for specification. For instance, we identify the semiconductor industry as the market sector in the framework. The hierarchical modeling levels of interest are the structure and elements utilized in the production process (e.g., machine tools, operators).

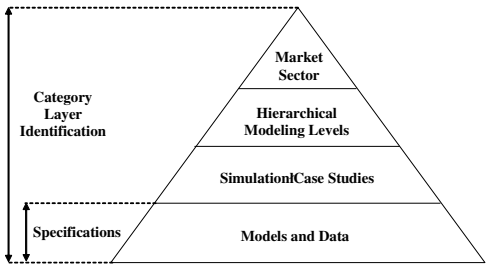

Figure 2: Hierarchy in the Proposed Framework for Standard Modular Simulation (adapted from McLean and Leong 2002)

Before specifying the models and data that will be required to build the simulation model, it is possible to identify the simulation case studies that will provide valuable support for decision-making in the fabrication operations. The process of designing the case studies can be considered as a recurrent process. In other words, after building a simulation model future modifications or adjustments could be necessary according to the simulation objectives. The layer of simulation case studies will provide the level of detail that the simulation model needs to provide, and therefore, will determine the structure of the models and data layer.

The last layer, corresponding to models and data, serves to identify and specify the items required to build the simulation model. For example, operations, resources, and production flows required in the production process can be specified in detail in this layer.

The following sections present details of the application of this framework for simulation of semiconductor fabs.

5 CATEGORY LAYER IDENTIFICATION: MARKET SECTOR, HIERARCHICAL MODELING LEVELS, AND SIMULATION CASE STUDIES

5.1 Market Sector: Semiconductor Industry

The first element of the proposed framework in (McLean and Leong 2002) is utilized to identify the market sector that corresponds in this case to the semiconductor manufacturing industry. The market sector identification is located on the highest layer of the framework, and it will determine the specification of the subsequent layers.

As mentioned in section 3, different simulation processes are conducted at different levels in the semiconductor industry. We focus our interest in an important area of simulation in the front-end process, which is the simulation of the semiconductor fab.

5.2 Hierarchical Modeling Levels: The Semiconductor Fab

The second layer serves to specify the levels of detail required in the modeling and simulation of the semiconductor fab. We consider the following levels:

- *Production Line:* Corresponds to the specification of the stations or *tool families* utilized in the production process and how the process flow is specified for each part produced in the fab.
- *Human Resources:* Process operators and maintenance technicians are considered human resources that are generally included in the modeling of semiconductor fabs.
- *Station:* In a semiconductor fab, stations are composed by a group of tools assigned to a specific operation (e.g., lithography, metal deposition) in the production process. Usually, these stations are integrated by tools that perform the same operation (e.g., tool families).
- *Equipment:* Machine tools or simply *tools* are the elements that integrate the stations. In semiconductor fabs, the tools are specialized equipment with different levels of complexity (e.g., from single to multiple chamber tools). Other equipment considered in this category are transporters (e.g., autonomous guided vehicles (AGV's)) and conveyors.
- *Process:* The lowest level in this hierarchical modeling specifies the operational parameters at the processing level in the fabrication tools (e.g., tool processing time, scheduling strategies, wafer starts per week, failure and repair statistics, probability distributions).

5.3 Simulation Case Studies in Semiconductor Wafer Fabrication

Simulation case studies are utilized to answer questions about how certain modifications in the current fab simulation model can affect the production performance (e.g., throughput, cycle time) (McLean and Shao 2003). From the general framework in (McLean and Leong 2002), we identified the following categories as potential components for a modular case study element in the simulation framework:

- *Scheduling:* the study of the effect of using different strategies to schedule jobs (e.g., dispatching rules (Panwalker and Iskander 1977))at the tool stations, also known as *shop floor control*, is a common question that can be answered with these type of case studies. For instance, see (Wein 1998, Kumar 1994, Narahari and Khan 1997, Rose 2001).
- *Plant Layout:* The impact of physical distribution of stations into the fab can also be subject to simulation experiments. For instance, travel times of materials between the stations and material handling can be analyzed, and different configurations of fab layouts can be evaluated through simulation case studies (e.g., (Campbell and Ammenheuser 2000)).
- *Capital Equipment:* the effect of variation in capital equipment can be analyzed under simulation case studies. These experiments can be used to evaluate variations in production capacity as well as in costs related with the production process (Grewal, Bruska, Wulf, and Robinson 1998). For instance, simulations can be performed to evaluate the economic impact of replacing tools with different failure probability distributions (e.g., different Mean Time Between Failures (MTBF)).
- *Work Force*: Operators and/or workers are usually modeled in semiconductor fab models. Therefore, the analysis of the impact of changes in workers schedules (e.g., availability), skill levels (e.g., providing training), contract workers, etc.; can provide useful scenarios for decision-making.
- *Product Mix:* in many semiconductor fabs the production is diversified and several products are produced. Questions that can be answered by this case study can be: What release rate or input regulation strategy is utilized with product mix?
- *Process Capability:* evaluation of production capabilities is important in semiconductor fab operations to project workloads as well as to evaluate capacity expansion and allocation (Grewal, Bruska, Wulf, and Robinson 1998, Bhatnagar, Fernandez-Gaucherand, Fu, He, and Marcus 1999).
- *Material Handling:* Advances in computer graphic animation and simulation tools have made possible the study of the effect of material handling (e.g., Automated Material Handling Systems (AMHS), Autonomous Guided Vehicles (AGV's)) in simulation of semiconductor fabs (e.g., (Campbell and Ammenheuser 2000)).
- *Maintenance:* One of the major sources of stochastic events in a semiconductor fab is tool downtime due to failures (Uzsoy, Lee, and Martin-Vega 1992). Reliability of the tools can be increased by applying appropriate preventive maintenance (PM). Therefore, PM scheduling strategies can be evaluated through simulation case studies (e.g., (Yao, Fernandez-Gaucherand, Fu, and Marcus 2004, Ramírez-Hernández and Fernandez-Gaucherand 2003)).

Other case studies mentioned in (McLean and Leong 2002) that can be included in this list are: *Capacity Analysis, Line Balancing, Cost Estimation, Process Validation, Tolerance Analysis, Ergonomic Analysis, Tooling,* and *Inventory*. The list presented above is by no means complete, but it represents a good selection of case studies commonly addressed in the semiconductor industry.

6 SPECIFICATIONS: MODELS AND DATA

The lowest layer in the proposed framework specifies the model and data required to implement the simulation case studies. One important objective towards the standardization of simulation procedures in the semiconductor industry will be the standardization in the format of model description in digital formats (e.g., data files). NIST is currently working on exchange formats for models and data utilized in simulation of manufacturing systems; for instance, see (Lee and McLean 2003). This effort is focused on generating exchange file formats using Unified Modeling Language (UML) and eXtensible Markup Language (XML). These efforts are part of the NIST's SIMA program described in section 2.

We follow the data structure proposed by McLean & Leong (McLean and Leong 2002) from which we selected the data elements that are generally required to specify a semiconductor fab model. In addition, we proposed an additional component denominated *Simulation Control Specifications.* The proposed structure for the models and data layer is composed of the following six elements: *(1) General Specifications*, *(2) Resource Definitions*, *(3) Product and Process Specifications*, *(4) Production Operations*, *(5) Layout*, and *(6) Simulation Control Specifications*.

The following subsections present details about each element according to the semiconductor fab modeling and simulation context.

6.1 General Specifications

For modeling and simulation of semiconductor fabs this group of data provides information about:

- *Model Revisions:* this segment of data is utilized to keep tracking of modifications and/or updated data in the model.
- *Data Set Summary:* description or summary of the key features of the simulation model.
- *Modeler Comments:* this section can be utilized by the modeler or analyst to include specific details about conditions for the simulation study (e.g., simulation length, replications, other specific conditions).
- *Units of Measurement:* the units utilized throughout the model are specified in this segment. For instance, in simulation models of semiconductor fabs the following are units commonly used:
  - Wafers and wafer lots to specify the units being processed by tools.
  - Seconds, minutes, and hours as time units.
  - Meters for distance units (e.g., fab layout specifications).
  - Combination of the above units can be utilized to specify other quantities; for instance the throughput rate in a tool could be specified in wafers/hour, or the meter/second to specify the speed of a transporter utilized to deliver material between stations.
- *Probability Distributions:* this set of data is utilized to specify the type of probability distribution for the random events in the production process. For instance: tool processing time, product arrival rates, tool failures times (e.g., Mean Time Between Failures (MTBF) or Mean Time To Fail (MTTF)), and Tool repair times (e.g., Mean Time To Repair (MTTR)).
- *Performance Metrics:* these are indexes that are utilized to measure production performance through simulation case studies. The following are some commonly used metrics in semiconductor manufacturing processes (Kumar and Kumar 2001): costs, cycle time, machine utilization, yield, and Work-In-Process (WIP) inventory.

6.2 Resource Definitions

Details about the resources required in the production process are identified in this structure. In the case of a semiconductor *fab*, the following could be a specification of this structure.

- *Resources:*
  - Manufacturing Tools: tool stations, number of tools per station, and Mean Time Between Failure (MTBF) or Mean Time To Fail (MTTF) specifications per tool.
  - Production operators and preventive maintenance technicians
  - Transporters (e.g., autonomous guided vehicles, conveyors, human-based transporters): number of transporters, associated tool stations, and physical specifications (e.g., speed, distance covered).
  - Other material handling devices (e.g., robots)
- *Skill Definitions:* maps the skill levels of operator or technicians with the corresponding process activities (e.g., level of training received).
- *Operations Definitions:* Defines the operation type per tool station (e.g., lithography, etching).

6.3 Product and Process Specifications

In general, product mix specifications are indicated in this level and could include the following structures:

- *Parts:* define the type of products fabricated in the fab and includes the number of products, associated production sequence (i.e., route or process flow per product), and lot size per product.
- *Process Plans:* specifies the work flow per product or routing, and other special operations in the production process. Step-by-step sequence or route:
  - Step identification (e.g., production step ID number).
  - Resources required: tool and processing time (e.g., probability distribution parameters), and number of operators required.
  - Batch size if batching operations are required at the current processing step in the sequence.
  - Setup, loading, and unloading times.
  - Rework percentage and rework re-routing specification.
  - Yield percentage.
  - Travel times to the next station/step sequence.

6.4 Production Operations

The data structures in these levels provide details about calendars of operative activities and work operations in the fab.

- *Calendars:* identifies shift schedules for operators, and breaks that can be represented as worker's availability maps.
- *Work:* this structure can be utilized to specify scheduling data or strategies followed for production control (e.g., shop-floor control). For instance:
  - Wafer starts per month (e.g., lot release rate, arrival time probability distribution) or input regulation strategies (e.g., Constant WIP (CONWIP) (Wein 1998, Rose 2001)).
  - Dispatching rules or scheduling strategies per tool station.

6.5 Layout

This section presents the physical distribution of the different elements that integrate the semiconductor fab (e.g., tool stations, transporters, parts transportation paths). This structure *"...defines the location of reference points within the site or facility, area boundaries, paths, and part objects. It contains reference pointers to external graphic files that may use appropriate graphic standards to further define these elements"* (McLean and Leong 2002).

Definition of the fab layout and its utilization with graphic interfaces are mainly utilized for animation purposes. For instance, this can be directly applied to the study of Automated Material Handling Systems (AMHS) strategies and equipment allocation in the shop floor (e.g., evaluate the impact in production performances from different layout configurations). For more details see (Campbell and Ammenheuser 2000, Lee and McLean 2003).

6.6 Simulation Control Specifications

An important piece of information about the simulation model are the details for running the simulation. This section includes details about simulation length, warm-up periods, number of replications, and other details relevant to the control of the simulation runs. This information is valuable for future validation and verification of the model if it is implemented under different simulation engines. Validation and verification is a key step in the simulation process that is beyond the presentation of the proposed framework for simulation. Useful guidelines and procedures for verifying and validating simulation models are presented by Law & Kelton in (Law and Kelton 2000).

The next section presents an example that illustrate how the proposed simulation framework is utilized to provide the necessary information required for modeling and simulating of a semiconductor fab. The example presented in the next section corresponds to one of a series of case studies and examples presented in (Li, Ramírez-Hernández, Fernandez, McLean, and Leong 2005).

7 EXAMPLE: INTEL FIVE-MACHINE MINI-FAB BENCHMARK

In this section we present an example of the application of the proposed simulation framework discussed in sections 4, 5, and 6. This example corresponds to a simple configuration of the *Intel Five-Machine Six Step Mini-fab* benchmark (Kempf 2005, Tsakalis, Flores-Godoy, and Rodriguez 1997).

We depart from the Models and Data layer in the proposed framework. We assume that the other layers in the framework have been properly specified in section 4. In addition, a simple simulation case study about the impact of the work force in the fab production performance is presented in the last subsection. The objective of this simulation example is to illustrate a specific type of case study that can be performed according to the proposed simulation framework and the *Mini-fab* model.

7.1 General Specifications

The following are the general specifications for the *Mini-fab*:

- *Model Revisions:*
  - Neither maintenance technicians nor operator's breaks are modeled in this model version.
  - Also, no buffer sizes are modeled for the tool stations.
  - Preventive Maintenance is not modeled.
  - Batch of lots can be mixed in any combination of products.
- *Data Set Summary:*
  - This is a five-machines six-step manufacturing process.
  - There are 3 different products in which one of them is a test product.
  - This model does not include rework nor travel times.
  - An operator is always required for loading and unloading the tools. During the time that the machine is processing the operators are not required.
- *Units of Measurement:* wafer lots is the unit being processed by tools and minutes and hours are the time units.
- *Probability Distributions:* both tool processing time and product arrival rates are deterministic while tool failures and repair times follow a uniform distribution.
- *Performance Metrics:* cycle time and WIP level.

7.2 Resource Definitions

Tables 1, 2, and 3 show details about the resources utilized in the *Mini-Fab* model.

Table 1: Tool Stations for the *Mini-fab* Model

Stations	Tool Name
1	Ma
	Mb
2	Mc
	Md
3	Me

7.3 Product and Process Specifications

The *Mini-fab* model has the following specifications for product and process:

Table 2: Operators for the *Mini-fab* Model

Stations	Operator Name
1	PO1
2	PO1, PO2
3	PO2

Table 3: Tool Station Failures and Repair Statistics for the *Mini-fab* Model

Station	MTTF (h)	MTTR (h)
2	U(24,76)	U(6,8)

U(a,b): Uniform distribution in the interval [a,b].

- *Parts:*
  - Number of parts (products): 2 standard products (Part 1, Part 2) + 1 testing product (TW).
  - Product associated production sequence or route: 1 unique sequence or process flow for every product.
  - Lot size per product: the basic unit is lots, therefore there is no lot sizing specification.
- *Process Plans:* Table 4 presents the process plan that consists of the tool stations, corresponding processing step, and processing time. In addition, Table 5 shows the setup, batching, load, and unload details per station.

Table 4: Process Plan for the *Mini-fab* Model

Station	Step	Processing Time (min)*
1**	1	225
	5	225
2	2	30
	4	50
3	3	55
	6	10

*Processing time is for units of lots.

**The given processing time for Station 1 is per batch.

7.4 Production Operations

The following are the details for production operations in the *Mini-fab* model.

- *Calendars:* operations are 24 hours, 7 days. A day-work is divided in two shifts of 12 hours each
- *Work:*
  - Wafer starts: Part 1: 51 lots per week; Part 2: 30 lots per week; and TW: 3 lots per week.

– Dispatching rules or scheduling strategies per stations: First-In-First-Out (FIFO).

Table 5: Setup, Load, Unload Times, and Batching Specifications for the *Mini-fab* Model

Station	SU	LD	ULD	BS
1	–	20	20	3
2	–	15	15	1
3	10	10	10	1

SU: Setup time (min), LD: Load time (min), ULD: Unload time (min), BS: Batch size (lots)

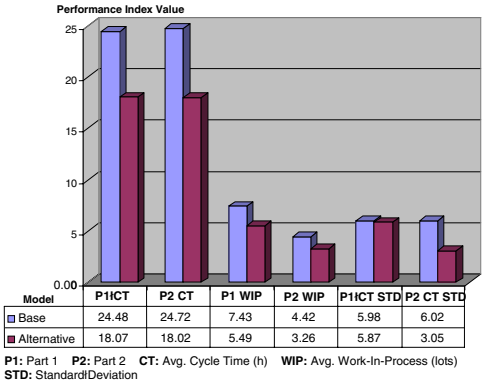

Figure 3: Performance Indexes for the Base and Alternative Models of the *Mini-fab*

7.5 Simulation Control Specifications

The simulation case studies consisted of 5 replications with a simulation length of 20000 hours and a warm-up period of 10000 hours.

7.6 Simulation Case Studies: Impact of Work Force in Production Performance

In this simple example, the *Mini-fab* model was utilized to compare the impact in production performance when an operator is added into the process. We consider the base model according to the definitions for this model previously presented in this section. The alternative system corresponds to a model including an extra operator. In other words we define the number of operators in the alternative systems as follows: 2 operators type PO1 + 1 operator PO2.

The simulation engine utilized to implement the model and perform the simulation runs was AutoSched AP (Phillips 1998, Brooks-Automation 2005). In addition, the simulation conditions are the same as those indicated in the subsection of Simulation Control Specifications.

Figure 3 depicts the values for the performance indexes resulting from the simulation results.

The results clearly indicated that an improvement in the cycle time and reduction in the average WIP levels are obtained by adding one more operator in the fab. The cycle time is decreased about 6 hours in average for both products, while the average WIP level is reduced in about two lots for product 1, and one lot for product 2. Also, the variation in the cycle time is reduced as it is indicated in the standard deviation values for the cycle time.

Other examples of the application of the proposed simulation framework, where larger simulation models are considered, are presented in (Li, Ramírez-Hernández, Fernandez, McLean, and Leong 2005).

8 SUMMARY

An application of a framework for standard modular simulation (proposed by NIST) of semiconductor fabs has been presented. A preliminary list of elements that integrate this framework in the context of modeling of semiconductor *fabs* have been discussed. The list of elements presented is by no means considered complete and further additions are possible. The specific application of the proposed framework was illustrated by presenting an example of the semiconductor fab model *Mini-fab*. In this example, a case study in work force impact in production performance was also presented.

Extension and improvement of the proposed framework is possible and necessary. For instance, an important factor to consider is how technological changes could affect the utilization of the standard. A preliminary answer for this question can be the application of an active updating process. Therefore, technological changes in the semiconductor manufacturing industry will be considered by updated versions of the standard. Similarly, other issues such as the levels of detail required in the modeling and simulation need to be reviewed carefully.

Currently, our efforts are being conducted in the identification and development of generic case studies for simulation of semiconductor wafer fabrication and the improvement of the proposed framework.

DISCLAIMER

The simulation case studies presented in this paper were conducted using AutoSched AP (Phillips 1998, Brooks-Automation 2005) as the simulation tool. This does not imply recommendation or endorsement by the authors or NIST, nor does it imply that this simulation tool is necessarily the best available for the purpose.

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