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AN ANALYSIS: TRADITIONAL SEMICONDUCTOR LITHOGRAPHY VERSUS EMERGING TECHNOLOGY (NANO IMPRINT)

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ABSTRACT

The introduction of emerging technologies into existing manufacturing facilities is not necessarily encouraged by the people responsible for the output of the facilities. Any "new" technology carries risks and people responsible for delivering manufactured products are, by nature, risk-adverse. This paper demonstrates the advantage of evaluating the impact of attempting to introduce a new technology into an existing facility before actually attempting the introduction. The first part of the analysis examines the impact on the total product delivery for a comparable volume of two facilities, one with the traditional processes and one with the new process replacing existing ones. Based on these results, a conclusion can be reached if there are sufficient benefits to consider pursuing the development and introduction of the new techniques. An example is employed that evaluates the introduction of nano-imprint.

1 INTRODUCTION

The Semiconductor Industry has been following a technology acceleration curve that is referred to as Moore's Law. The curve in Figure 1 indicates the growth of the number of transistors in a unit area of 1cm2. While this doubling of density every 2 to 3 years is impressive, the realm of physics that is being entered into is even more impressive. This shrinkage of feature size has definite markers or identifiers for the feature size and is based on 70% shrinkage in linear dimension every three years or less. The 70% shrinkage results in an area reduction of 50% every three years. To keep things understandable, the feature size becomes the measure of a generation. In the mid 1990s, the feature size was defined as 250nm or ¼ micron. That means that the minimum dimensions for lines and spaces for dense (tightly packed) features was ¼ micron. That generation was followed by the 180nm generation, the 130nm one, and the current 90nm lines and spaces feature sizes.

The minimum feature size that can be produced by an optical system is equal to K1*lambda/NA, where K1 is a factor that has a theoretical limit of 0.25. The first approach that was employed was to reduce the wavelength of light and it has progressed from 365nm (I-line) to 248nm and now is at 193nm. In the last 20 years the Numerical Aperture (NA) has increased from less than 0.5 to the current 0.93 through material and design enhancements. In order to keep shrinking feature sizes, alternatives have been investigated. 157nm illumination was evaluated and shelved due to material requirements that were beyond the capability of existing technology.

The future is challenging with the 90nm generation being followed by 65nm, 45nm, and 32nm in the next few years. The process of creating the semiconductors involves creating multiple levels of circuitry with the transistors at the bottom and the interconnect layers at the upper levels. An example of the issues that are arising can be demonstrated by considering the upcoming 65nm generation. The feature size of the gates (the basic part of the transistor) will be 25nm! The light that is used to create the current features is 193nm. This means that these feature sizes will be approximately 1/8 the wavelength of the light employed to create them. This is a non-trivial challenge. While optical engineering has provided significant advances in capabilities of exposure systems, even these enhancements appear to be approaching a limit. Since 1996 there has been significant effort in developing alternative or next generation lithography (NGL) technologies.

The time it takes to produce a production worthy new technology is another consideration. The development cycle of a new lithographic technology has taken a minimum of eight years. The technology consists of the fundamental tool, the patterning device (traditionally an optical mask with the patterns), the resist (where the patterns are formed), and associated infrastructure elements to provide a viable manufacturing platform. The development efforts required are non-trivial. It is estimated that the cost to the industry for the development of Extreme UltraViolet

(EUV) technology will be in excess of $7.6B. The development costs for making the 193nm technology production worthy was in excess of $2.5B (Trybula and Newberry 2004).

In the last two years an alternative approach has been developed. By employing a liquid between the optical system and the wafer with the semiconductor device, the NA can be increased. NAs of 1.30 to 1.35 now appear to be possible. There are even development efforts underway to increase the NA to greater than 1.5. Alternative technologies, like EUV with a wavelength of 13.5nm are being developed for the future manufacturing. Then there are non-optical approaches, like nano imprint, that are also vying for the opportunity to become the next technology that will be inserted into manufacturing. How can the selection be made?

2 CHALLENGE

Consider a specific example to understand the evaluations that must be undertaken. The current state of the existing 193nm technology indicates that there will be some manufacturing challenges at the 45nm generation for 193nm lithography. This opens opportunities for EUV to fill the need. However, the timing for the 45nm generation is 2009, which may challenge the ability to have the technology manufacturing ready. The 32nm generation, which is two years later, is less time constrained.

While there has been substantial progress made in developing newer technologies for the very leading edge applications, the impact of the feature size shrinkage is that moderate size features are now becoming sub wavelength. These features become harder (consequently more expensive) to implement in manufacturing.

In addition to the efforts in EUV, there has been substantial progress in the nano imprint technology. This is an approach that creates an impression in the resist-like material to create the patterns. While this technology is a relative new-comer to the industry, it has some strong claims about being more cost effective than other approaches. How can we evaluate the impact on production of technologies that are not developed?

2.1 Specific Example

While there has been substantial progress made in developing newer technologies for the very leading edge applications, the impact of the feature size shrinkage is that moderate size features are now becoming sub wavelength. These features become harder (consequently more expensive) to implement in manufacturing.

The 65nm generation is expected to have between 38 and 40 layers for leading edge logic. This translates into over 600 processing steps. The interconnection layers are really a layer for each pair of conductors. The conductor on the bottom needs to have a connection to the layers above it. Typically, this connection or via layer is the size of the conductor on the bottom. Figure 1 shows the level build up of the circuitry. Due to the use of illumination to stabilize the "resist" the process is knows as Step and Flash Imprint Lithography (SFIL).

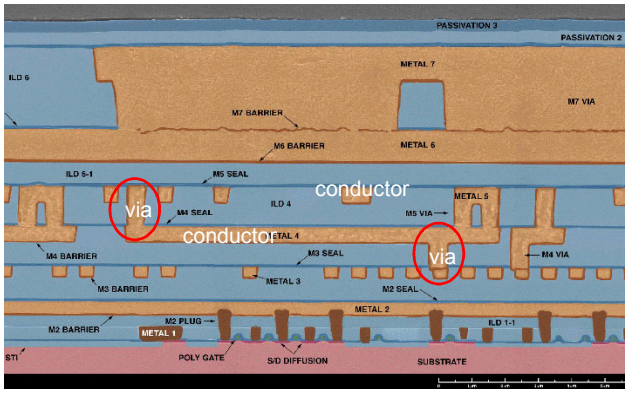

Figure 1: Level of Circuitry (Courtesy IBM)

Currently there is a process, nano imprint, being proposed for rapid insertion into the manufacturing environment. The claim is that it will provide significant cost savings and provide an efficient process for manufacturing semiconductors. The process involves replacing the optical process with an imprint process (SFIL-r) as shown in Figure 2. An additional concept is the development of a process that actually produces two layers simultaneously, and is called the dual damascene process (SFIL-d2).

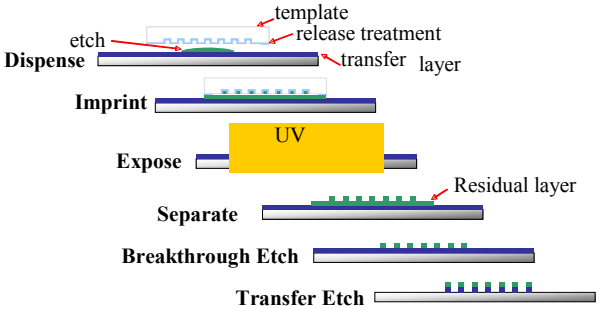

Figure 2: SFIL Process Flow

The ability of the nano imprint process (SFIL-d2) to actually make both conductor and via level in one processing step has provided incentive to evaluate the potential of nano imprint. If it were possible to reduce the number of steps from 24 to 8 for each of the eight metal layers, the savings would be 128 process steps out of slightly more than 600 processing steps. Figure 3 show the comparison of the optical process and the dual damascene process (Stewart et al. 2005).

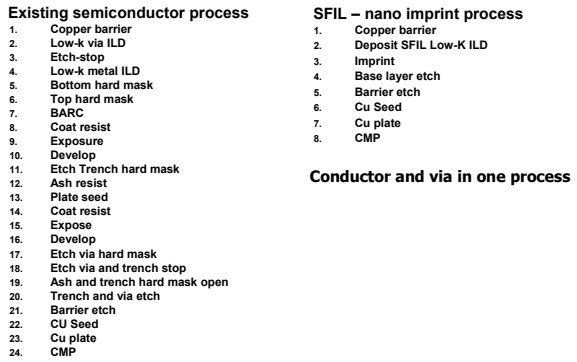

Figure 3: SFIL-d2 and Optical Process Flows

Obviously, there is potential for significant savings. This raised the question, "How much saving could be expected for implementing nano imprint?"

3 INFORMATION REQUIRED

What needs to be understood is the impact on the existing process if nano imprint were introduced into manufacturing. How much savings would be generated? What would be the impact on cycle time?

The issues that arise with projected technological insertion are that there are a large number of unknowns. At the early development stage of a technology only estimates are available for equipment throughput, maintenance, supplies, etc. The cost of both the imaging masks and the resist are unknown for both cost and operating conditions. An example of this is evidenced by values published in (Wright William and Kelly 2004) that present the imprint mask (template) as being about 35% of the cost of an optical mask. In an ongoing SEMATECH study (Hector 2005) the cost of the template is 92% of the optical mask. Since the mask costs can approach and even exceed $100K each, this is a non-trivial difference (Trybula 2001). There are other examples of potential projections that can not be proved until equipment is developed, debugged, and made fully operational.

The approach is to perform a modeling analysis on the proposed technology and compare it with a similar analysis of the existing technology. By employing a range of variables, it is possible to create a range of expected values that should provide enough information to bracket the plausible answer.

4 MODELING EFFORTS

The modeling effort needs to deliver an answer on the potential cost impact on the manufacture of wafers. There are two complimentary approaches that are employed within SEMATECH and ISMI. The first approach is a static modeling efforts that is based on the Cost of Ownership (CoO) model and the Cost Resource Model (CRM) that were developed by SEMATECH in the mid 1990s. Every wafer generation since 350nm has been modeled with these tools. The output of the modeling effort includes the total number of each type of equipment required, the cost of each layer, and the total cost of the finished wafer.

4.1.1 Static Modeling

Factory level cost modeling (CRM) was performed making comparisons for the 65nm (high performance logic) node for optical, SFIL-d2 (two layers simultaneously) and SFIL-r (replacing only one optical level). More specifically, the analysis centers around the modeling of metal levels 5 –7 and compares the cost of processing these metal levels using optical photolithography with 248nm DUV equipment to that of Imprint tools and imprint technology process steps for the same metal levels. Additional comparisons are made to the use of 193nm dry and immersion equipment. Table 1 shows the Imprint equipment assumptions. The throughput is given in terms of wafers per hour (wph). In either cases, the mask life is assumed to be 4000 wafers per mask.

Table 1: Equipment Assumptions

Flow	Cost	wph	Resist (\gallon)	Resist usage (\wafer)	Mask template cost
SFIL-d2	$5M	15	$12K	0.7 ml	30,000
SFIL-r	$5M	12	$8K	1 ml	50,000

The resulting cost of each metal level can be seen below in Table 2. The SFIL-d2 process yields the greatest savings in process costs indicating a 51% decrease in costs whereas the SFIL-r process yields a savings in processed cost of 20% per metal level when one compares the cost of 248nm processing versus imprint lithography.

Table 2: Cost per Metal Level

Flow	Cost of metal levels 5-7	Total processed wafer cost	Number of process steps
SFIL-d2	149	3,998	542
SFIL-r	246	4,281	617
248nm	306	4,413	608

When comparing the results of overall total processed wafer cost, SFIL-d2 and SFIL-r each result in a savings of 9% and 3% respectively. The capital cost assumptions for this modeling assume a $14M capital cost for 248 DUV and an effective throughput of 35 wafers per hour. Correspondingly, the imprint equipment was modeled at a cost of $5M with a throughput of 12 wafers per hour (SFIL-d2) and a slightly faster throughput of 15 wafers per hour for the SFIL-r process. The cost comparison of the metal lev-

els as well as the total processed wafer cost consider equipment depreciation and maintenance, materials, personnel, and building depreciation.

Table 3: Processing Costs

Wafer Processing Costs	SFIL	SFILr	Optical
Tool Depreciation	1,492	1,606	1,658
Tool Maintenance	522	562	580
Direct Personnel	32	35	34
Indirect Personnel	24	26	26
Direct Space	313	340	340
Indirect Space	10	11	11
Direct Material	1,171	1,222	1,254
Indirect Material	434	479	509
Total Cost	**3,998**	**4,281**	**4,413**

Table 3 shows a summary of all processing costs. As expected, materials and equipment related expenses are the major contributors to overall processing cost. The SFIL process has the advantage of reduced number of process steps and thus requires 11% less equipment capital to manufacture the 20k wafer starts per month, common across all models.

4.1.2 Dynamic Modeling

While the results of the static modeling are promising, there area still unanswered questions about actual quantities of equipment and cycle time. With the cost of construction of cleanroom space of $4,000 per square foot and annual costs of $750 per square foot, the size required for the equipment is important. The discrete event simulation model was built using AutoSched Accelerated Processing™ (ASAP) v 8.0, an object-oriented modeling tool. This effort builds on the previous models that have been validated with existing manufacturing facilities.

The key findings from this analysis is that the cycle time for the three imprint dual damascene layers is reduced from 82.5 hours to 65.5 hours or a decrease of seventeen hours. Considering that a number of the process steps that are eliminated are non-queueing, non-capacity limited operations, it is not surprising that the reduction is small.

5 CONCLUSIONS

The first conclusion is that there is an apparent significant reduction in the both cost and cycle time by inserting the dual damascene process. This is an incentive to push the technology forward at as fast a pace as possible. Since there is the potential for significant savings, the savings will vary depending on the actual values that the equipment can achieve and the related costs of mask and material. However, this potential is great enough that further efforts are warranted. The SFIL-r process indicates that there would be a savings, but the difference is not very large and could be reduced with the technology development process delivering actual results that have much less optimistic values.

The effect of employing simulation, both static and dynamic, provides a means of evaluating the impact of new technology. By coupling the modeling with cost analysis, a measure of the potential for the technology can be developed along with an assessment of risk. While it is not possible to develop an accurate measure of a technology that is not developed, bounds can be created that provide an indication of the anticipated returns.

Future work will be directed at an analysis of employing the imprint process for an increasing number of layers, as well as resolving the cost recovery time for a new process that has a lower yield at its introduction than an established technology.

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WALT TRYBULA, Ph.D., MBA, IEEE Fellow, is a Senior Fellow at SEMATECH in Austin, Texas. At SEMATECH, Dr. Trybula's current activities involve the emerging technologies in both semiconductors and nanotechnology. His most recent published emphasis is on nanotechnology, cleaning/contamination issues, and patterning with both charged particle maskless and nano imprint. Walt has been active in promoting nanotechnology importance to the Industry and the community. He has presented the need for building the evolving nanotechnology infrastructure to the U.S. Senate Staff in June 2003, taught "Introduction to Nano Technology" courses at the 2004 ECTC and the 2004 IEMT conferences, is on the Board of the Texas State University's Nano-materials Application Center, and was active in developing the first SEMI Nano-Forum and Workshop in 2004. He is currently the co-chair of the Texas State Strategy on Advanced Technology for both the nano-technology technical working group and the

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RANDAL K. GOODALL received his Bachelors of Science in physics from Caltech (1977) and his Masters (1979) and Ph. D. (1984) in experimental solid-state physics from the University of Oregon. In early 1994, Randy joined SEMATECH as a Senior Member of Technical Staff in the Silicon Materials group on some of the earliest 300mm efforts at SEMATECH. IN 1995 he was one of six members of the startup team for the International 300 mm Initiative (I300I). In 1998, the I300I programs merged with International SEMATECH, and in 2000, Randy was named associate director of a new Manufacturing Methods and Productivity division, focusing on productivity for existing and future fabs and equipment. He subsequently developed the Texas Technology Initiative (TTI) and worked with the governor and other state and local officials to pass 2003 legislation which included the formation of the Advanced Materials Research Center. As the first Director of the newly-formed External Programs office, Randy is providing leadership in 2005 for SEMATECH, the TTI, the State Strategy on Advanced Technology, and the proposed $300M Texas Emerging Technology Fund. Dr. Goodall has published numerous papers on silicon wafer technology, collaborative industry transitions, including 300mm wafers, and productivity modeling. He continues to engage local, state, and national government efforts to drive technology innovation and economic development, and he works with technology leaders, university administrators and researchers, and State officials to fulfill the vision of the TTI.