Proceedings of the 1999 Winter Simulation Conference
P. A. Farrington, H. B. Nembhard, D. T. Sturrock, and G. W. Evans, eds.

CRITICALITY OF DETAILED MODELING IN SEMICONDUCTOR SUPPLY CHAIN SIMULATION

Sanjay Jain
Chu-Cheow Lim
Boon-Ping Gan
Yoke-Hean Low

Gintic Institute of Manufacturing Technology
71 Nanyang Drive
SINGAPORE 638075

ABSTRACT

Supply chain management offers a large potential for organizations to reduce costs and improve customer service performance. Simulation of supply chains can help in these objectives by evaluating the impact of alternate inventory control policies. Supply chain simulation involves modeling of multiple factories across the chain and can get quite complex. Analysts typically carry out such simulation at a coarse level of detail to keep the complexity and computing resources manageable. However, modeling at coarse levels may reduce the accuracy of outputs and affect the quality of decisions. In this paper, we report on a study to compare the quality of results at different levels of details in a semiconductor supply chain simulation.

1 INTRODUCTION

The globalization of markets is forcing the producers to look for ways to improve their competitive positions through focusing on supply chain management. Supply chain management involves planning and managing the flow of material and information through multiple stages of manufacturing, transportation and distribution until it reaches the customer. It includes planning of replenishments of incoming inventory at each manufacturing stage. It includes planning of operations at each manufacturing stage. It includes planning of shipments for products from one stage to the next. Some of these components of supply chain, in particular the operations planning, have been the focus of productivity improvement efforts. However, the improvements made locally have not always contributed to global improvements in the supply chain performance. The replenishment planning and shipment planning components offer large opportunities for improvements. These "soft" costs spread throughout the distribution channels provide the easier target for effecting savings (Magretta 1998). The key is to study the overall system to plan the inventory, production and transportation activity through the supply chain.

The need to model the supply chain is particularly critical in semiconductor industry. Semiconductor wafer fabrication facilities represent large capital investments, usually in the range of US$1-1.5 Billion. The assembly and test facilities are quite expensive also with some of the individual testers costing more than US$1 Million. The products generated from these facilities are of high value, both in the form of wafers and in the form of integrated circuit (IC) chips. In case of processor chips, each unit can be of the order of few hundred US Dollars. With these high capital investments and cost of products, it is critical for semiconductor manufacturers to maintain high utilization of the equipment with minimal inventory. Supply chain management can help in achieving these goals and provide large savings for the semiconductor industry.

The need to simulate and redesign supply chain processes to allow decision makers to explore various options and scenarios that are customer and value driven has been recognized (Hennessee 1998). Some of the early development and uses of supply chain simulation are being reported from corporate centers and research organizations. IBM has developed its own supply chain simulation tools and have used them for substantial improvements in the performance of their internal supply chains (Bagchi et al. 1998). IBM Industry Solutions Unit is also using the tools for its clients. While many of the existing simulation software can be used as a platform for building supply chain models, there isn't any tool available commercially that provides pre-built features for this purpose. Early developers are charting their own definitions and scope of the supply chain simulation tools.

One of the major issues in the creation of supply chain simulation is the level of detail that each of the links in the

chain should be modeled at. In any simulation study, the level of detail modeled depends on the purpose of the effort. With the focus on supply chain performance, the level of detail for the manufacturing stages varies among different efforts. Heita (1998) models manufacturing stages as having constant capacity and a fixed throughput time in supply chain simulation. Umeda and Jones (1998) model manufacturing facilities in detail down to cell level with associated control logic simulations in a test-bed system for supply chain management. Multiple manufacturing cells, buffers, and material handling operations are modeled. A third approach takes the middle of the road approach though it has not been reported in the context of supply chain simulation. This approach is based on Theory of Constraint concepts, and reduces the complexity of simulation models by modeling only the bottleneck workstations while the other processes are modeled as delay (For examples in semiconductor manufacturing, see Rose 1998, and Peikert, Thoma and Brown 1998).

The different levels of detail involve widely different level of efforts in building the model. Is the effort to build a detailed model of the manufacturing stages within the supply chain simulation required? Does the level of detail of modeling these stages significantly affect the output results of the supply chain model? This paper attempts to answer these questions with respect to a defined scenario by modeling the manufacturing facilities in a supply chain simulation at two different levels of detail and comparing the results.

The next section describes the supply chain simulation model used for the study. Section 3 describes the simulation engine used for the study. The two levels of details are elaborated on in Section 4. Section 5 describes the experiments and the results of the comparisons. Section 6 draws conclusions from the results and closes the paper with directions for future work.

2 SEMICONDUCTOR SUPPLY CHAIN MODEL

It was mentioned in the introduction that supply chain simulation development is still in early stages and the scope is defined differently in various efforts. The following basic elements are included in different efforts.

- **Manufacturing**. At least two successive stages of material transformation in manufacturing facilities should be modeled. That is, at least one link of the chain needs to be modeled.
- **Transportation**. The transportation of material between successive manufacturing stages should be modeled.
- **Business Processes**. Basic processes to be included are forecasting, production and inventory planning. The forecasting process models the procedures used by an organization to determine demand forecasts. The production and inventory planning processes model the policies used for control of material flow through the successive manufacturing stages. This will include the production lots released based on the target inventory levels in between the manufacturing stages.
- **Customer Orders**. The actual consumption of products at a rate usually different from the forecasted rate needs to be modeled to represent real life situation.

The supply chain model used in this study comprises of these very basic elements. A supply chain scenario in semiconductor manufacturing comprising of multiple wafer fabrication facilities supplying to an assembly and test facility is modeled as shown in figure 1. The scenario is perhaps better described as a "supply network", since it models multiple parallel flows instead of one single flow suggested by a "supply chain", or as a "supply link", since it models only two successive stages of production. The wafer fab plant data is based on Sematech dataset 5, a dataset representing a logic and ASIC wafer fab. The dataset describes a real wafer fab in operation and was contributed by one of the member companies of Sematech. It is available together with other datasets through the Internet (MASMLab 1999). The assembly and test facility dataset is a representative set representing a logic and ASIC environment based on our past projects with the industry. The matching of wafers to IC products was developed based on volume considerations; that is, large volume wafer products supply the large volume IC products. The transportation of wafers from fabs to the assembly and test facility is modeled as a short delay typical of the industry.

To improve customer service, semiconductor enterprises aim at reducing their lead times by keeping strategic products in inventory. These products are either determined by forecasts or by business agreements with strategic customers, specified as intents before placement of the firm order (Makatsoris et. al., 1996). Also, a limited amount of excess is produced to protect against yield variations. For the supply chain model in this study, the wafer fab production is on a make-to-stock basis driven by forecast, while the assembly and test production is on a make-to-order basis. The choice is also driven by the cycle times. The wafer fab cycle times range from 3 to 10 weeks (Atherton and Atherton 1995) while the assembly and test cycle times are in the order of a few days (for examples, see NS Electronics Bangkok 1997 and WTEC 1997). It is reasonable to assume that a customer will wait for a few days to get delivery of his order, the time for assembly and testing of the ICs. However, the customer cannot be

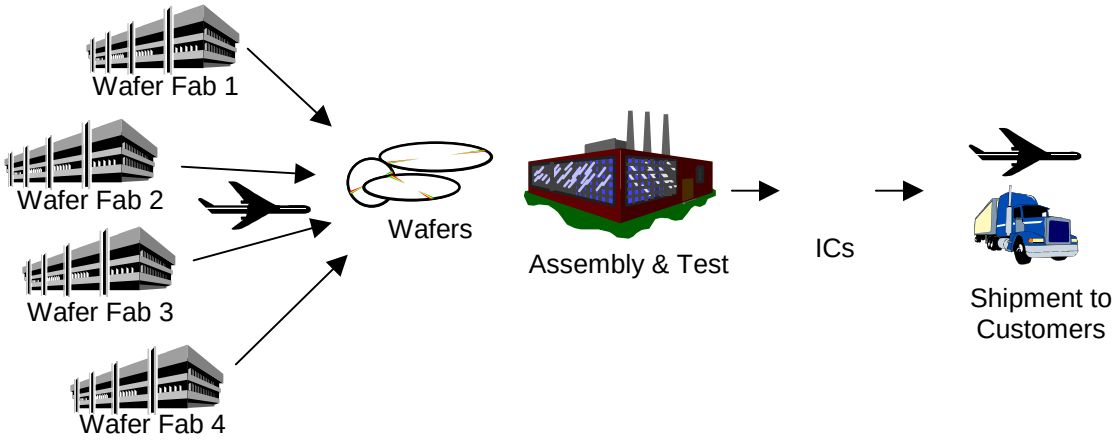

Figure 1: Scope of Semiconductor Supply Chain Considered in this Study

expected to wait for the long time that will be incurred if the production is initiated at the wafer fab after receipt of the order. The approach used here is simple but provides a reasonable representation of semiconductor industry operation.

The lot release in the wafer fabs in the study is based on the forecast for the period of product consumption. For example, if a product has a two month cycle time through the wafer fab, the quantity released in *n*th month in wafer fab will be based on the forecasted consumption for *(n+2)*th month. The forecast is based on the average monthly quantity with a random distribution. In addition to the forecast for the target period, the current inventory level and the work in progress level is taken into account to determine the adjusted release quantity. The lot release in assembly and test facility is driven by actual customer order arrivals. The arrivals themselves are based on a set of actual monthly orders repeated with random arrival patterns.

The interactions between the components of the semiconductor supply chain model are summarized in Figure 2. Only two wafer fabs are shown for ease of presentation. The figure shows the information flows using solid lines and material flows using dashed lines. Each factory has a business sub-model and a manufacturing sub-model.

An assembly and test facility's business sub-model gets information on the current wafer inventory, and sends it back to the wafer fab's business sub-model (for the latter's planning). It also models receipt of the orders (based on order arrival and quantity distributions) and lot release for the assembly and test facility's manufacturing sub-model. We use the following rule to assume that existing stock is available for the lots at the beginning of the assembly and test's manufacturing sub-model simulation. Suppose a lot for product *k* uses wafer product *j*. We must check if there is sufficient product *j* stock to

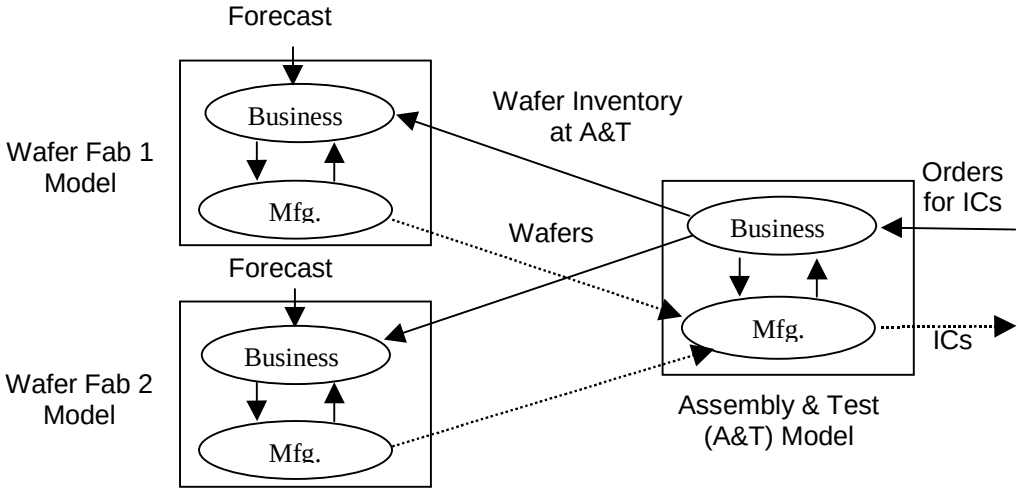

Figure 2: Interactions between Components of Semiconductor Supply Chain Model

release a product-*k* lot. If there is insufficient stock, a product-*k* lot is delayed until further shipment arrives from any of the wafer fabs. However, during the warm-up period, as long as the assembly and test facility has not received any lot for product *j*, we assume that there is sufficient stock for a product-*k* lot to be released immediately. After the first wafer product *j* lot arrives at *T*, we continue to assume sufficient stock until one month after *T*. This rule helps to start up the model without having a large number of lots waiting for release at assembly and test.

A wafer fab's business sub-model receives the assembly and test facility's stock information, and keeps track of the amount of work-in-progress within its own manufacturing sub-model. It also forecasts the demand for each wafer product. We have used a simple formula to adjust the forecast to determine the actual release quantity.

Let,

N_j	=	cycle time in months (≥ 1) for product *j* ,
$D_{j,m}$'	=	forecast demand for product *j* for the $(m+N_j)$th month at the beginning of m^{th} month.
$d(j,m,N_j)$	=	sum of forecast demands for m^{th}, $(m+1)$th, ….$(m+N_j-1)$th months for product *j*
wip(j)	=	current work-in-progress in number of wafers in wafer fabs
inventory(j)	=	current excess stock in numbers of wafers at the assembly and test facility
$e_{j,m}$	=	excess wafers for product *j* at beginning of m^{th} month
$R_{j,m}$	=	adjusted release rate for m^{th} month

The business model next considers whether there might be any excess wafers from the (forecast) demands.

$$e_{j,m} = wip(j) + inventory(j) - (j,m,N_j).$$

Then, the adjusted release rate for product *j* in month *m* at the wafer fab is determined as:

$$R_{j,m} = D_{j,m}' - e_{j,m}$$

The maximum release rate for each product is bounded to four times the average release rate to avoid clogging the manufacturing facilities. Capacity planning processes will be modeled in future to control the release rate based on policies used in the industry.

3 SIMULATION ENGINE

The simulation engine used for this study is a sequential discrete event simulator developed in C++ under a joint project of Gintic Institute of Manufacturing Technology and School of Applied Science of Nanyang Technological University, Singapore. The project is aimed at developing parallel and distributed simulation (PADS) for implementation of virtual factory concept. The virtual factory concept proposes integration of models of sub-systems, such as manufacturing, business processes and communication networks (Jain et al. 1998). The sequential discrete event simulator has been developed for performance comparison with the parallel simulator developed under the project.

The parallel simulation effort is targeted at the semiconductor manufacturing industry. Currently the manufacturing simulation capabilities of the simulators are based on the features defined in Sematech Modeling Data Standards (MDS) (Sematech 1997). The simulators read in the data from files defined in the Sematech MDS format. Most of the features defined in the Sematech datasets have been provided for in the simulators. The input file structure for the simulators has been extended beyond the Sematech MDS format for the purpose of accommodating the capability of modeling assembly and test facilities. The simulation capabilities for each feature are first built and verified in the sequential model and then moved to the parallel simulator. The sequential simulator thus provides a rigorous performance benchmark and a verification tool for the parallel simulator. The two simulators have been validated against commercial simulation tools with executions of common datasets.

In addition to the manufacturing simulation capabilities, the simulators also have features to model business processes described in the section 2 above. Also, the simulator has the capability to model a single facility, multiple independent facilities or multiple facilities linked in a supply chain. The scope of the overall simulation is defined using parameter files while individual facilities are described using the MDS format files.

An MDS data set is made up of a number of files. The process route file contains information for one or more process routes (or work flows). The file lists the processing steps of each route, according to their order in the route. The information for each step is stored in a record, and includes the machine and operator required for that step, the average amount of processing time etc. There are two resource files in an MDS data set: one for tool (machine) sets and one for operator sets. Each record in the tool set file specifies the number of machines in the set, plus additional information about down time etc. Similarly, each record in the operator set file specifies the number of operators in the set, plus other information e.g. break-time etc. The volume release file describes, for each product, the process route it uses and its rate of arrival.

To make the manufacturing sub-model realistic, we model two types of machines. (a) A lot-processing machine processes a wafer lot at a time. (b) A batch machine groups several lots into a single batch for processing.

Each machine set has dispatch and setup rules to decide how a wafer lot is to be assigned to a free machine in the set. A dispatch rule is used to order the waiting wafer lots. One example is the first-come-first-served rule that gives higher priority to a lot which has been waiting for a longer time. For an example of setup rule, consider a machine set consisting of two multi-functional machines, each of which can process either of two steps *S'* or *S"*. Suppose one machine is currently set up to process a lot at step *S'* and the other for *S"*. If a wafer lot now arrives to be processed at step *S"* and the machine with the right setup for *S"* is busy, but the other is idle, should the lot be assigned to the idle machine? This will involve an overhead (in terms of simulated time) to change its setup from *S'* to *S"*. The setup rule determines if the wafer lot should wait for the busy machine or force a setup change in the idle machine. A machine is required to remain in the same setup for a minimum period of time before its setup can be changed. This is to prevent wasting time in changing setup repeatedly. Lots, which have exceeded their maximum waiting time, always have higher priority.

4 LEVELS OF DETAIL IN SUPPLY CHAIN MODELING

The supply chain simulation (SCS) was carried out in two levels of detail for the manufacturing facilities. The business sub-models remain the same in all our experiments.

SCS with bottleneck only manufacturing models ($SCS_{bottleneck}$). In this case, the manufacturing models are summarized to consider only the bottleneck machines and attending operators as constrained resources. The bottleneck machines are determined for each process route based on their utilization level. For the results reported in Section 5, we take the note that each route may have multiple bottleneck machines. The time for a lot to travel through non-bottleneck machines, including process time, set-up times, queuing times, and travel times are put together as delay steps. For the reentrant flow in wafer fabs, the process plan collapses into a much shorter plan with steps on bottleneck machines interspersed with delay steps for all the other steps.

SCS with detailed manufacturing models (SCS_{detail}). In this case all steps in the process plan are modeled with all machines and operators (where defined) considered as resource constraints.

The simulator itself does not require any modification for modeling at the two selected levels of detail. As described above the changes are done through the data files only. Specifically, only the process flow file is modified to change from the fully detailed flow to bottleneck steps and delay steps flow.

5 EXPERIMENT AND RESULTS

The experiments in this study compared the SCS with bottleneck only manufacturing models ($SCS_{bottleneck}$ models) against the SCS with detailed manufacturing models (SCS_{detail} models). Each model consists of four wafer fabs supplying wafer lots to a single assembly and test facility. Multiple runs are made for each level with different random streams to determine the performance in each case with a certain level of confidence. We conducted simulation runs for the SCS_{detail} and $SCS_{bottleneck}$ models for periods of 300, 600 and 900 days. Each run is repeated five times with different random streams.

We will first compare the SCS_{detail} and $SCS_{bottleneck}$ models in terms of several statistics and then argue that the SCS_{detail} models present information which is missing from $SCS_{bottleneck}$ models. It is therefore worthwhile to do SCS modeling at the detailed level. This is particularly the case when the system (i.e. the supply chain) may not be in a state of equilibrium and has dynamic behavior that cannot be easily captured by simple statistics e.g. mean and standard deviations.

The primary objective of supply chain management is to achieve the right balance of customer responsiveness and low inventory levels with an aggressive cycle time (Turcotte et al. 1998). It involves using synchronized production, inventory and transportation plans to keep low cycle times. The performance measures of interest in supply chain management, hence, are customer service level, inventory level and product cycle times.

The customer service level is defined as the percentage of lots that are completed within the due date. The due date is dependent on the order date and average cycle time of the product. Let T be the theoretical minimum cycle time of a product k. When the first attempt to release a product-k lot is at time t, its expected due date is computed as $t + 4T$. This is within the quoted cycle time range of 3 to 10 times of theoretical process time in the industry (Atherton and Atherton 1995). If the lot's release is delayed due to insufficient stock, the expected due date is *not* postponed. Short cycle times enable an organization to quote early promise dates to a customer and thus provide a competitive edge. Cycle times of some of the major products are also analyzed in this study. The service levels of the models are presented in Table 1.

There seems to be a significant difference in the prediction of the service levels of the wafer fabs using either SCS_{detail} or $SCS_{bottleneck}$ models. This difference diminishes over a long simulation period (in our case, 900 days). It might seem to suggest that for long simulation periods, $SCS_{bottleneck}$ is sufficient without the detailed modeling, but the other statistics strongly argue otherwise.

The service levels of the wafer fabs with bottleneck modeling are much higher than with the detailed modeling for the 300-day simulation period. If a decision is based on the bottleneck modeling results, the decision makers of the assembly and test facilities will opt to carry a lower amount of inventory than required. This will lead to inventory shortages and consequently delays in meeting customer orders.

The inventory throughout the supply chain should remain low without starving the bottleneck stages and affecting the service levels. Of particular interest is the inventory in-between the manufacturing stages. In our study, we focus on the wafer inventory in the die bank at the assembly and test facility (Table 2). For the SCS_{detail} model, the average amount of inventory decreases over a longer simulation period. This is not observed on the $SCS_{bottleneck}$ model (inventory increases on 600 days run). The detailed SCS models consistently predict a lower level of inventory than the corresponding $SCS_{bottleneck}$ model.

We next present statistics on the cycle times of the first wafer fab and the assembly and test facility from both SCS_{detail} and $SCS_{bottleneck}$ models for 300, 600 and 900 days (Table 3). The data is presented for a few selected high volume products.

We also examine how the cycle times of a large-volume product vary over the simulation period for both SCS_{detail} and $SCS_{bottleneck}$ models. At both levels of details, there is a cyclical pattern to the cycle times, but the patterns are vastly different (Figure 3).

In each graph, we compare the cycle time variations predicted by SCS_{detail} and $SCS_{bottleneck.}$ The horizontal lines are computed from 4X CT where CT = theoretical cycle time of a lot for product 8.

From the tables 1-3, it can be seen that the two sets of results are quite different. The underlying thesis is that the detailed modeling option provides more accurate results, and may present quite different information about the supply-chain's dynamic behavior from that in $SCS_{bottleneck}$ models (e.g. cyclical pattern in the lot cycle times of product 8 in our experiments). It is therefore worth the extra time and effort to do detailed modeling.

6 CONCLUSION

The results highlight the need for executing supply chain simulations with fully detailed model of the component links. Use of abstracted models for supply chain simulation can potentially lead to inaccurate determination of the needed inventory levels for maintaining desired customer responsiveness. The inaccuracy in this important item of information can lead to erroneous decisions hurting a company's performance. It may be critical to model the manufacturing activity at a detailed level in scenarios that are similar to the semiconductor supply chain examined here.

The results here are based on a hypothetical supply chain even though the individual stage datasets are based on real facilities. Given the hypothetical scenario, the results cannot be validated against the real system. It is highly recommended that supply chain simulations be validated against real supply chain performance to ensure the correctness of results. The research team is looking for industry partners to verify the conclusion on more data sets and implement these concepts.

Table 1: Service Levels (Percentage of Lots Completed by Due Date) in Supply Chain Simulation (SCS) at Different Levels of Details

Run Length →	**300 days**		**600 days**		**900 days**	
Model	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$
Wafer fab 1	0.780	1.0	0.718	1.0	0.646	0.930
Wafer fab 2	0.806	1.0	0.678	0.955	0.658	0.898
Wafer fab 3	0.879	1.0	0.742	1.0	0.725	0.958
Wafer fab 4	0.809	1.0	0.683	1.0	0.666	0.928
Assembly & test	0.656	0.479	0.676	0.462	0.656	0.455

Table 2: Inventory at the Assembly and Test Facility (Number of Wafers) in Supply Chain Simulation (SCS) at Different Levels of Details

Run Length →	**300 days**		**600 days**		**900 days**	
Measure	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$
Average	25865.8	34827.5	23930.5	37380.3	21707.0	34680.7
Std. Deviation	8447.2	12319.3	6666.3	9150.3	6371.1	8578.4

Table 3: Mean Cycle Times (in Minutes) of the Lots in Supply Chain Simulation (SCS) at Different Levels of Details

Run Length →		**300 days**		**600 days**		**900 days**	
Wafer fab 1 Product	**Measure**	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$
Pdt 8	Mean	47473.3	38667.4	54726.3	41753.5	60289.8	46054.8
	Std dev	21664.9	10536.0	20650.3	11331.8	21276.6	15649.4
Pdt 14	Mean	45201.8	35634.6	51157.8	39235.8	55996.3	43445.3
	Std dev	21589.4	10577.0	20935.7	11455.7	20637.2	15694.1
Pdt 15	Mean	58648.4	43385.6	67956.1	47565.0	75096.0	51856.2
	Std dev	26034.5	10723.3	26835.9	11592.8	28260.1	15732.0

Run Length →		**300 days**		**600 days**		**900 days**	
Assembly & Test Product	**Measure**	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$	SCS_{detail}	$SCS_{bottleneck}$
Pdt 520	Mean	942.7	944.1	938.6	939.3	939.5	937.6
	Std dev	114.7	104.5	95.9	81.6	90.0	72.0
Pdt 701	Mean	5407.5	6788.1	4422.9	6784.0	4287.9	6784.2
	Std dev	706.9	291.3	1170.4	285.2	1298.2	283.3
Pdt 864	Mean	24674.9	23986.6	45064.4	44108.1	64295.8	64115.1
	Std dev	11582.4	11601.6	23212.6	23098.0	33871.8	34591.8

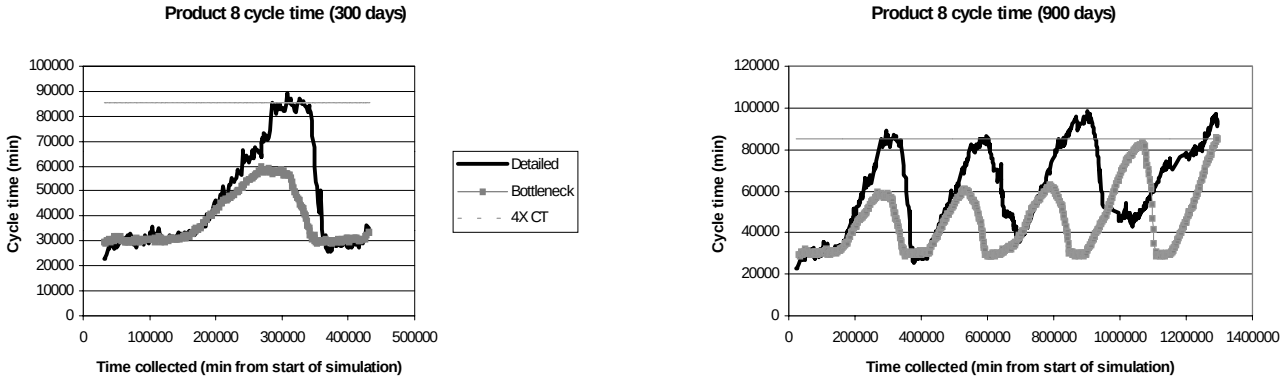

Figure 3: Variations of Cycle Times of a Large-Volume Product for Simulation Periods of 300 and 900 Days

Using supply chain simulation with fully detailed manufacturing models, as supported by this study, will result in models that consume long amount of execution times. Parallel simulations that can reduce the execution times will be particularly useful for supply chain simulations. The parallel simulator developed under the project cuts down the execution times from 10% to 50% reduction using a 4 CPU Sun Enterprise 3000 (250 MHz UltraSparc2) (Lim et al. 1998). Efforts will continue to develop the parallel simulation for providing more consistent performance.

In the future, it is anticipated that potential partners will evaluate formation of supply chains using simulations. This will be facilitated by partners being able to integrate their respective models for the purpose across the Internet. The parallel simulation concepts will be extended to a distributed execution framework for enabling such partnership explorations.

ACKNOWLEDGEMENTS

This research is supported by National Science and Technology Board, Singapore, under the project: Parallel and Distributed Simulation of Virtual Factory Implementation. It is a collaborative project between Gintic Institute of Manufacturing Technology, Singapore and the School of Applied Science in Nanyang Technological University (NTU), Singapore. The project resources are currently located at the Center for Advanced Information Systems at NTU.

REFERENCES

Atherton, L.F., and R.W. Atherton. 1995. *Wafer Fabrication: Factory Performance and Analysis*. Kluwer Academic Publishers.

Bagchi, S., S.J. Buckley, M. Ettl, and G.Y. Lin. 1998. Experience Using the IBM Supply Chain Simulator. In *Proceedings of the 1998 Winter Simulation Conference*, ed. D.J. Medeiros, E.F. Watson, J.S. Carson and M.S. Manivannan, 1387-1394. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.

Hennessee, M. 1998. Challenges Facing Global Supply-Chains in the 21st Century. In *Proceedings of the 1998 Winter Simulation Conference*, ed. D.J. Medeiros, E.F. Watson, J.S. Carson and M.S. Manivannan, 3-4. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.

Hieta, S. 1998. Supply Chain Simulation with LOGSIM-Simulator. In *Proceedings of the 1998 Winter Simulation Conference*, ed. D.J. Medeiros, E.F. Watson, J.S. Carson and M.S. Manivannan, 323-326. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.

Jain, S., N.F. Choong, K.M. Aye, and L. Ming. 1998. Towards Implementing a Virtual Factory. In *Proceedings of Rensselaer's International Conference on Agile, Intelligent and Computer Integrated Manufacturing*, Electronics Agile Manufacturing Research Institute, Rensselaer Polytechnic Institute, 110 Eighth Street, CII Building, Room 9009, Troy, NY 12180-3590, USA.

Lim, C.C., Y.H. Low, B.P. Gan, S.J. Turner, S. Jain, W. Cai, W.J. Hsu, and S.Y. Huang. 1998. A Parallel Discrete-Event Simulation of Wafer Fabrication Processes. In *Proceedings of the High Performance Computing Conference*, 1180-1189. Institute of High Performance Computing, Singapore.

Magretta, J. 1998. Fast, Global and Entrepreneurial: Supply Chain Management, Hong Kong Style - An Interview with Victor Fung. *Harvard Business Review*, Sept-Oct 1998, 103- 114.

Makatsoris, C., N.P. Leach, H.D. Richards, C.B. Besant, and M. Ristic. 1996. Addressing the planning and control gaps in semiconductor virtual enterprises. In *Proceedings of the Conference on Integration in Manufacturing*, Galway, Ireland.

MASMLab. 1999. TestBed [Online], maintained by Modeling and Analysis of Semiconductor Manufacturing Laboratory, Industrial and Management Systems Engineering department, Arizona State University, USA. Available: http://www.eas.asu.edu/~masmlab/ftp.htm [1999, February 1].

NS Electronics Bangkok. 1997. Advantages to do business with NSE [Online]. Available: http://www.nseb.com/advant.htm [1999, July 2].

Peikert, A., J. Thoma, and S. Brown. 1998. A Rapid Modeling Technique for Measurable Improvements in Factory Performance. In *Proceedings of the 1998 Winter Simulation Conference*, ed. D.J. Medeiros, E.F. Watson, J.S. Carson and M.S. Manivannan, 1011-1015. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.

Rose, O. 1998. WIP Evolution of a Semiconductor Factory after a Bottleneck Workcenter Breakdown. In *Proceedings of the 1998 Winter Simulation Conference*, ed. D.J. Medeiros, E.F. Watson, J.S. Carson and M.S. Manivannan, 997-1003. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.

Sematech 1997. Modeling Data Standards, Version 1.0. Technical Report, Sematech Inc., Austin, TX 78741.

Turcotte, J., B. Silveri, and T. Jacobsen. 1998. Are You Ready for the E-Supply Chain? *APICS-The Performance Advantage*, Volume 8, Number 8.

Umeda, S., and A. Jones. 1998. An Integration Test-Bed System for Supply Chain Management. In *Proceedings of the 1998 Winter Simulation Conference*, ed. D.J. Medeiros, E.F. Watson, J.S. Carson and M.S. Manivannan, 1377-1385. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.

WTEC. 1997. Electronics Manufacturing in the Pacific Rim [Online] Appendix C. Singapore Site Reports - ST Assembly Test Services (STATS). Available: http://itri.loyola.edu/em/toc.htm [1999, July 2].

AUTHOR BIOGRAPHIES

SANJAY JAIN is a Senior Research Fellow and the Manager of the Manufacturing Planning and Scheduling group at Gintic Institute of Manufacturing Technology, Singapore. His research interests are in the area of using modeling and analysis techniques in development and operation of manufacturing systems, and in improving performance of simulation systems through parallel and distributed execution. Prior to joining Gintic, he worked for several years as a Senior Project Engineer with General Motors North American Operations Technical Center in Warren, MI, U.S.A. He received a Bachelors of Engineering from the University of Roorkee, India in 1982, a Post Graduate Diploma from National Institute for Training in Industrial Engineering, Bombay, India in 1984, and a PhD in Engineering Science from Rensselaer Polytechnic Institute, Troy, New York in 1988. He is a member of the Institute of Industrial Engineers and serves on the editorial board of the *International Journal of Industrial Engineering*.

CHU CHEOW LIM is a Senior Software Engineer at Intel Corporation. Prior to this, he was a Research Fellow with the Manufacturing Planning and Scheduling group in the Gintic Institute of Manufacturing Technology, Singapore. From 1994 to 1997, he was with the Defense Science Organization, Singapore, as a Project Engineer. He received a B.S. in Mathematical and Computational Sciences and M.S. in Computer Science from Stanford University, California (1987 and 1988 respectively), and Ph.D. in Computer Science from University of California at Berkeley (1993). His research interests include parallel computing, simulations, compilers and e-commerce.

BOON-PING GAN is an Associate Research Fellow with the Manufacturing Planning and Scheduling group at Gintic Institute of Manufacturing Technology, Singapore. He received a Bachelor of Applied Science in Computer Engineering and Master of Applied Science from Nanyang Technological University of Singapore in 1995 and 1998 respectively. His research interests are parallel programs scheduling, parallel discrete event simulation, and genetic algorithms.

YOKE-HEAN LOW received the BASc in Computer Engineering from Nanyang Technological University, Singapore in 1997. He is currently a Research Associate with the Gintic Institute of Manufacturing Technology, Singapore. His research interests include parallel discrete event simulation and parallel processing. He is a member of the IEEE.