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SCHEDULING MEMS MANUFACTURING

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ABSTRACT

This paper focuses on the production scheduling in MEMS (Micro-Electro Mechanical System) manufacturing. The whole MEMS production process can be organized into 3 sub-processes, i.e., the wafer front-end process, the wafer cap process and the back-end process. Every wafer processed by the wafer front-end process needs to be bonded with a wafer that is manufactured in the wafer cap process, and then it will be sent to the back-end process. Therefore how to synchronize the release of wafers into the front-end process as well as the wafer cap process becomes an important topic. An ineffective coordination will create long cycle time and large WIP (work-in-process). In this paper, four synchronization rules are developed and they are evaluated together with two release rules and five dispatching rules. The performance measures considered are cycle time, throughput rate and WIP. A visual interactive simulation model is constructed to imitate the production line. The simulation results indicate that synchronization rules, release rules, and dispatching rules, have significant impacts on the performance of MEMS manufacturing and the best policy combination is Littlesyn-CONWIP-SRPT.

1 INTRODUCTION

MEMS (Micro-Electro Mechanical System) is integrated micro devices or systems combining electrical and mechanical components fabricated using integrated circuit (IC) compatible batch-processing techniques and range in size from micrometers to millimetres. These systems can sense, control, and actuate on the micro scale and function individually or in arrays to generate effects on the macro scale. MEMS can be used to provide robust and inexpensive miniaturization and integration of simple elements into more complex systems. Current MEMS applications include accelerometers, pressure, chemical, and flow sensors, micro-optics, optical scanners, and fluid pumps.

Since MEMS is the integration of mechanical substrate through the utilization of microfabrication technology, its processes combine IC processes with highly-specialized micromachining processes. The electronics components are fabricated using integrated circuit (IC) process sequences, while the micromechanical components are fabricated using compatible micromachining processes that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices. Therefore, the process flows and the equipment used in MEMS manufacturing are very similar to those for wafer fabrication, which is one of the world's most complicated manufacturing processes. The production flow of a wafer may re-enter the similar sequence of machine groups from layer to layer in its fabrication process. Owing to the re-entrance nature, wafers of different types as well as different layers of fabrication may compete for resource. Besides, there exist huge uncertainties in operation due to frequent machine failure and fluctuation of yield rate. Therefore, it is very challenging to develop sound scheduling rule in wafer fabrication. The same scenario will be expected in MEMS systems.

However, the MEMS production is not the same as wafer fabrication and has its own characteristics. The MEMS manufacturing studied in this paper is based on a commercial SCREAM (single crystal reactive etching and metallization) micro-machining technology. This technology uses reactive ion etching both to define and release structures (Mardou 1997). SCREAM portrays a relatively new micromaching approach and represents an important new technique from several points of view. It is a self-aligned, single mask process, run at low-temperatures ($<300^0$C), and completed in less than 8 hours that can be carried out in the presence of integrated circuitry on the same chip. This production process can be broken into 3 sub-processes, the wafer front-end process, the wafer cap process and the back-end process (see Figure 1). Raw wafers are processed in batches of 18 in the front-end process and the wafer cap process concurrently. One output

from the front-end process and one from the wafer cap process are bonded together and processed in the back-end process. In the back-end process, wafers are processed individually instead of in batches of eighteen. In the wafer front-end process, there are 106 steps and the sum of processing time is 62.2 hours. While in the wafer cap process, they are only 24 steps and 14.6 hours respectively. Since the output wafers from these two sub-processes will go through the bonding workstation, one of the critical issues is how to synchronise the release of these two sub-processes. If the synchronisation problem is not properly managed, the cycle time (the time from the release of the raw material to the production line until it comes out) of the product will become longer and more WIP will be resulted.

According to the authors' knowledge, there is currently no publication considering synchronization rules in MEMS manufacturing. However, we can find some studies on the similar scheduling problems. Avram and Wein (1992) considered the product design problem of allocating the chip sets on a semiconductor wafer to various types of chips. A stochastic analysis was employed to develop an effective wafer design, to measure the improvement in performance of the multitype wafer over the rate at which lots of wafers are released into the facility. Manfred M., Michael Purm and Ottmar G. (1995) proposed two sequencing rules (named set management policies) to synchronize prefabricated parts for assembly into modules in the multi layer ceramics (MLC) manufacturing lines. The results showed that these rules achieve better results than standard rules such as FIFO (first in first out) or EDD (earliest due date) both in the mean of cycle times and WIP levels and their variances. These papers can provide us with some insides to develop synchronization rules for MEMS manufacturing.

There have been a lot of studies on production scheduling in wafer fabrication. Wein (1988) evaluated the performance of four input rules and 12 different dispatching rules in a wafer fab using simulation and his results indicated that scheduling has a significant impact on average throughput time with larger improvements coming from discretionary input control. Also in this paper, he suggested an input rule called Workload Regulating (WR) rule. Glassey and Resende (1988a and 1988b) suggested a rule called Starvation Avoidance (SA) rule, in which a new wafer lot is released to avoid starvation of a bottleneck workstation. By simulation experiments, it showed that this rule gives a shorter flow time and a higher throughput rate than other rules. Mark L. Spearman, David L. Woodruff and Wallace J. Hopp (1990) described a pull based production control strategy CONWIP that offers the possibility of significant improvement over other production control systems and even Kanban. This seems to be particularly true at high levels of plant utilization and in environments with distinct bottleneck operations. Uzsoy, Lee, and Martin-Vega (1992; 1994) have also provided extensive surveys on production scheduling in wafer industry. These studies show that production scheduling can significantly improve the performance measures of wafer fabrication. Due to the similarity between MEMS manufacturing and wafer fabrication, these scheduling rules and research methods can also be applied in MEMS industry.

The purpose of this study is to develop scheduling rules to reduce cycle time and keep low WIP. Four synchronization rules, two release rules, and five dispatching rules are used to evaluate the performance of the MEMS manufacturing. Since the production flow in MEMS is very complicated, a discrete event simulation model is built to imitate its process flow. Simulation is a process through which a system model is evaluated numerically and the data from this process is used to estimate various quantities of interest. Although the "real world" systems do not conform to some assumptions made to simplify a model that is too complex to yield an analytical solution, the mathematical solution may still be valid. Thus simulation provides an alternative to test the scheduling heuristics on the production line without having to experiment with the real production line.

The remainder of this paper is organized as follows. Section 2 describes the scheduling rules applied in this study and the MEMS manufacturing models. In Section 3,

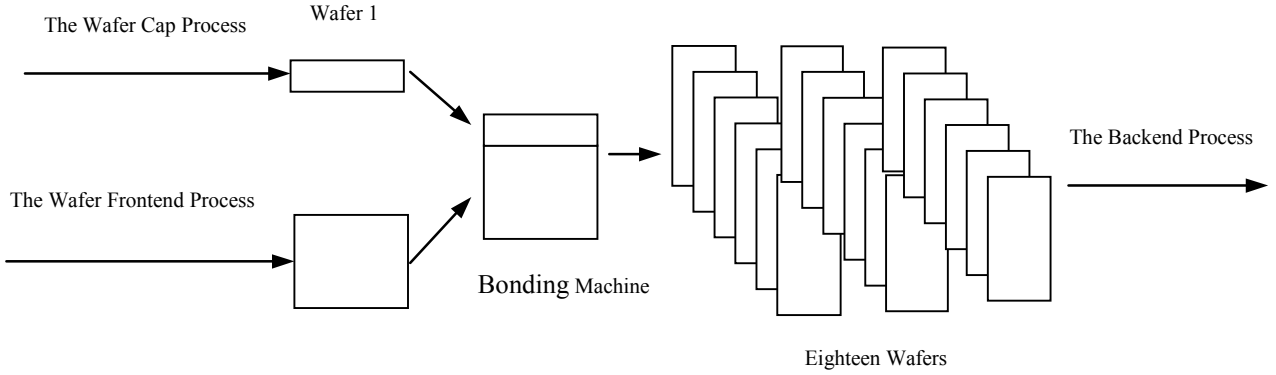

Figure 1: One Wafer (Wafer 2) Output from the Wafer Front-end Process and One (Wafer 1) from the Wafer Cap Process Are Bonded Together and then Divided into 18 Wafers

the results of this simulation study are presented and discussed, and the conclusions of the study are contained in Section 4.

2 SIMULATION EXPERIMENTS

2.1 The Scheduling Rules

Owing to its complexity, three types of scheduling rules are studied in MEMS manufacturing (see Figure 2). Since the wafer frontend process is the main part of the whole MEMS process, it will be easier to develop synchronization rules to control the release mechanism of the wafer cap process. Therefore, we use release rule to decide when to release a raw wafer into the wafer frontend process. After one wafer has been released into the frontend process, when to release a raw wafer to the wafer cap process is determined by the synchronization rule. Dispatching rules are used to decide which wafer waiting before a workstation to be processed first when the workstation is free in the whole process.

The following are two release rules considered in this paper:

Poisson Input: In this rule, when to release a raw wafer into the wafer frontend process is determined by the customer order. Once a product order arrives, a wafer will be released. Generally, the arrival of the product order follows the exponential distribution independent of the current WIP level.

CONWIP: Constant work-in-process, start a new wafer whenever a lot is completed. With this rule, throughput rate is controlled by the WIP level.

We have developed four synchronization rules for this MEMS process. The descriptions of them are as follows:

Simplesyn (simple synchronization): This is a simple way to release the wafer to the wafer cap process. One wafer will be released into the wafer cap process on the same time as a wafer is released to the front-end process.

Delaysyn (delayed-release synchronization): Since the sum of the processing time of the wafer cap process is much shorter than that of the front-end process, a natural thought is to delay the release to the wafer cap process. The extreme way is to release one wafer to the wafer cap process only when one wafer in the wafer front-end process arrives at the bonding workstation.

Wbsyn (workload balancing synchronization): In this rule we release the wafer to the wafer cap process so as to balance the workload between theses two sub-processes. As described previously, the MEMS production line is too complicated to be analyzed intuitively (see Figure 3). Therefore, at first, we will simplify the whole production line to be virtual flow shop which is shown in Figure 4. Since the total processing time of the cap process is 14.6 hours, we only need to observe the last portion of the front-end process whose sum processing time is around 14.6 hours. Then we will calculate the observed workload WR which is calculated by WIP level at the most bottleneck machines (indicated by A & B). Whenever *WR(B)* falls below *WR(A),* we will release one wafer into the wafer cap process.

Littlesyn (synchronization based on Little's Law): Let L_1, L_2 be the waiting length in the frontend process, the w- afer cap process respectively. Similarly, λ_1, λ_2, W_1, W_2, stand for the throughput rates and waiting times. Because of the bonding operation, the number of wafers output from the frontend process should be equal to the number of those from the wafer cap process in a relatively long time, i.e., $\lambda_1 = \lambda_2$. According to Little's law, $L=\lambda W$, we can get $L_1/W_1=L_2/W_2$. To keep the calculations simple, we take the waiting time for an individual wafer to arrive at the bonding workstation to be the sum processing times of all the operations with ignoring queueing and machine down time, i.e., $W_1=62.2$ and $W_2=14.6$. So whenever

$$L_1/62.2>L2/14.6,$$

we will release a new wafer to the wafer cap process.

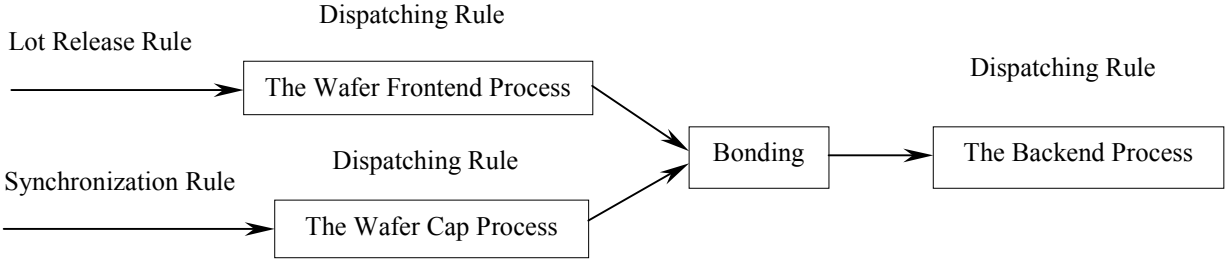

Figure 2: Schematic View of the MEMS Manufacturing Process and the Scheduling Rules

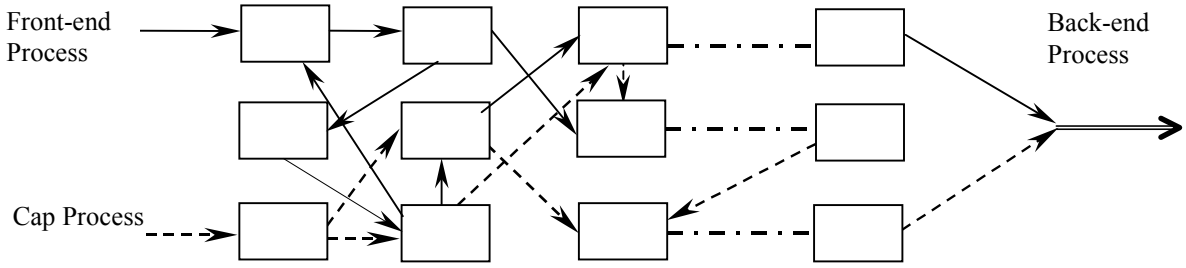

Figure 3: Schematic Representation of the Front-end Process and the Cap Process

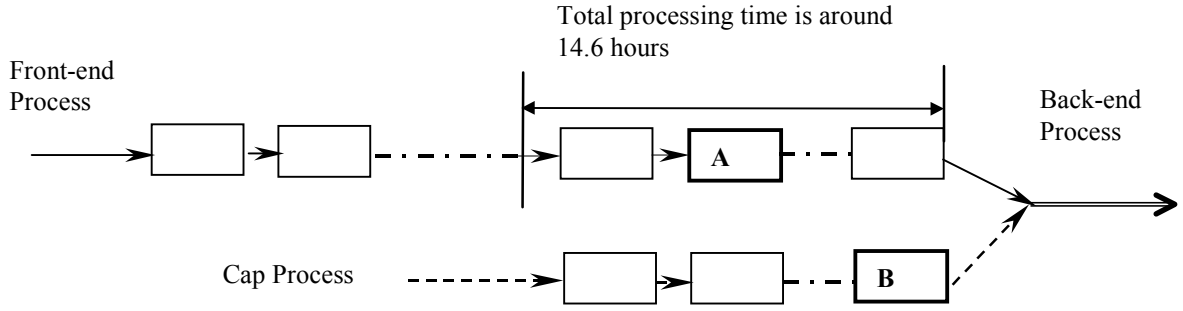

Figure 4: Schematic Representation of the Virtual Flow of the Front-end Process and the Cap Process

Also five dispatching rules are compared in this study. The descriptions of them are listed as follows:

- **FIFO**: First In First Out, dispatch the wafers in the same order as they enter the queue.
- **LIFO**: Last In First Out, dispatch the wafer last that enters into the queue first.
- **SRPT**: Shortest Remaining Processing Time, give priority to wafers with the least remaining processing time of all operations not performed.
- **LRPT**: Longest Remaining Processing Time, give priority to wafers with the most remaining processing time of all operations not performed.
- **EDD**: Earliest Due Date, dispatch wafers according to the due date of the wafers, the earliest due date will be dispatched first.

2.2 The MEMS Manufacturing Model

To compare the rules suggested in this study, a series of simulation experiments is performed. Performance measures used for the comparison are FRONTCT (cycle time for the wafer released into the wafer frontend process, the time from the release of the raw material to the front end process until it comes out from the back end process), CAPCT (cycle time for the wafer released into the wafer cap process, the time from the release of the raw material to the wafer cap process until it comes out from the back end process), product throughput rate, FRONTWIP (work-in-process in the front-end process), CAPWIP (work-in-process in the cap process) and TWIP (total work-in process in the whole process).

The MEMS manufacturing line considered in this study is relatively complicated. There are 106 steps in the front-end process, 24 steps in the cap process, and 18 steps in the back-end process. The manufacturing line consists of 38 single-server workstations. The bottleneck workstation is the spin rinse dry workstation, where a lot in the wafer frontend process before it is finished will visit 16 times and 5 times for that in the wafer cap process. For simplicity, we assume that there is only one type of MEMS product in the production line.

As described above, the bottleneck workstation-spin rinse dry station is highly burdened and apt to failure, so its parameter values include mean processing time, mean time between failure and mean time to repair. Comparatively, the other machines and stations have constant processing times since they are much lowlier utilized and do not breakdown so often. The processing time at the bonding workstation is ignored because it is much shorter compared to the others. Setup times are included in processing times since a machine can process the same types of lots for a long time and hence setups are very rarely done. The transfer time between workstations is negligible because it is much smaller than the processing time.

The release rate under Poisson input is 0.0855 lots/hour so that the throughput rate is kept around 1,500 units/hour and the single bottleneck station is highly utilized (about 90%). To approximate the throughput rate, the CONWIP input is chosen with the lot number of eight. When EDD rules applied, the due date data are generated

with an exponential distribution. The average value is 2000 hours which is similar to the actual data used in the company.

In the simulation experiments, four synchronization rules, two release rules and five dispatching rules which resulted in 40 combinations were to be investigated. Each case was run for 30 replications (runs) and each simulation was run for simulation time of 20,000 hours. Different random seeds were used for the 30 runs, and each run was started with an empty line. To obtain system performance in a steady state, statistics of the initial transient period (1,0000 hours) of each run were excluded from analysis. The simulation models are built using *EXTEND (version 4.01),* a simulation software developed by Imagine That Inc., USA. It is an object-oriented, user-friendly, advanced simulation tool for decision support.

3 SIMULATION RESULTS AND DISCUSSIONS

Results of the tests are summarized in Tables 1, 2 and Figures 5 to13. In table 1, both the average values and the

Table 1: Simulation Results under Poisson Release Rule

	FRONTCT (hours)	CAPCT (hours)	Throughput Rate (units/hour)	FRONTWIP (units)	CAPWIP (units)	TWIP (units)
Simplesyn-FIFO	299.44 (±53.8)	299.44 (±53.8)	1.5319 (±0.0301)	288.48 (±38.9)	270.56 (±38.9)	736.30 (±127)
Simplesyn-LIFO	314.28 (±31.0)	304.01 (±30.1)	1.5379 (±0.0208)	296.32 (±30.2)	278.37 (±30.2)	819.18 (±103)
Simplesyn-SRPT	222.64 (±24.1)	196.84 (±17.2)	1.5362 (±0.022)	296.24 (±31.4)	278.27 (±31.4)	622.22 (±72.3)
Simplesyn-LRPT	1240.0 (±215)	1233.5 (±216)	1.4841 (±0.0605)	591.75 (±115)	573.83 (±115)	2539.8 (±429)
Simplesyn-EDD	203.13 (±14.9)	200.00 (±14.3)	1.5521 (±0.0273)	249.05 (±20.3)	231.12 (±20.3)	570.14 (±55.1)
Delaysyn-FIFO	218.33 (±20.0)	178.62 (±13.6)	1.5303 (±0.0235)	254.99 (±29.5)	240.42 (±32.5)	605.76 (±73.3)
Delaysyn-LIFO	218.33 (±20.0)	163.62 (±13.6)	1.5323 (±0.0235)	254.90 (±29.5)	230.42 (±32.5)	600.71 (±73.3)
Delaysyn-SRPT	176.20 (±11.6)	67.412 (±3.60)	1.5368 (±0.0182)	240.85 (±17.5)	57.677 (±3.51)	325.87 (±21.9)
Delaysyn-LRPT	581.23 (±91.2)	442.23 (±64.0)	1.5495 (±0.0362)	432.67 (±48.5)	201.85 (±11.5)	1125.1 (±150)
Delaysyn-EDD	215.96 (±18.4)	209.32 (±14.4)	1.5293 (±0.0221)	249.78 (±21.8)	299.64 (±47.6)	645.82 (±81.0)
Wbsyn-FIFO	243.64 (±23.9)	141.27 (±17.3)	1.5337 (±0.0284)	277.49 (±23.0)	107.32 (±10.0)	483.38 (±51.1)
Wbsyn-LIFO	245.66 (±18.3)	157.15 (±14.9)	1.5430 (±0.0238)	263.79 (±18.3)	114.60 (±10.2)	508.02 (±42.1)
Wbsyn-SRPT	287.05 (±31.3)	106.53 (±9.32)	1.5385 (±0.0198)	269.40 (±41.3)	80.003 (±5.57)	518.79 (±56.0)
Wbsyn-LRPT	574.08 (±142)	416.89 (±122)	1.5429 (±0.047)	421.06 (±76.7)	204.07 (±40.3)	1128.7 (±351)
Wbsyn-EDD	248.34 (±23.2)	170.70 (±19.7)	1.5486 (±0.027)	293.71 (±26.8)	157.41 (±18.2)	571.87 (±66.0)
Littlesyn-FIFO	239.08 (±34.8)	123.72 (±19.6)	1.5608 (±0.0216)	269.38 (±33.5)	65.266 (±7.87)	445.60 (±63.9)
Littlesyn-LIFO	228.47 (±24.3)	126.16 (±15.9)	1.5381 (±0.0277)	243.29 (±23.3)	59.206 (±5.51)	445.20 (±57.6)
Littlesyn-SRPT	194.02 (±15.1)	84.783 (±6.01)	1.5523 (±0.0203)	264.30 (±21.0)	64.112 (±4.91)	370.30 (±31.2)
Littlesyn-LRPT	551.91 (±94.4)	381.50 (±65.5)	1.5041 (±0.0365)	398.26 (±89.6)	95.314 (±21.1)	977.28 (±191)
Littlesyn-EDD	206.89 (±16.0)	108.16 (±13.3)	1.5456 (±0.0236)	247.88 (±22.2)	60.363 (±5.29)	405.26 (±46.4)

Table 2: Simulation Results under CONWIP Release Rule

	FRONTCT (hours)	CAPCT (hours)	Throughput Rate (units/hour)	FRONTWIP (units)	CAPWIP (units)	TWIP (units)
Simplesyn-FIFO	112.83	112.83	1.5259	135.00	117.00	289.21
Simplesyn-LIFO	118.73	102.19	1.5094	135.00	117.00	295.25
Simplesyn-SRPT	114.23	76.351	1.4931	135.00	117.00	282.14
Simplesyn-LRPT	122.34	115.87	1.5391	135.00	117.00	303.80
Simplesyn-EDD	116.16	101.06	1.5074	135.00	117.00	292.61
Delaysyn-FIFO	113.31	125.13	1.5278	135.00	153.00	317.12
Delaysyn-LIFO	118.77	83.505	1.5092	135.00	85.919	256.05
Delaysyn-SRPT	114.36	50.494	1.4964	135.00	44.034	201.93
Delaysyn-LRPT	122.15	110.06	1.5413	135.00	140.43	318.39
Delaysyn-EDD	116.41	93.173	1.5152	135.00	103.51	271.13
Wbsyn-FIFO	113.80	52.730	1.5113	135.00	43.673	209.73
Wbsyn-LIFO	120.68	60.532	1.4769	135.00	50.658	220.32
Wbsyn-SRPT	114.49	46.422	1.4994	135.00	37.427	199.26
Wbsyn-LRPT	123.73	81.332	1.4938	135.00	68.893	247.98
Wbsyn-EDD	121.47	62.602	1.4955	135.00	55.362	225.01
Littlesyn-FIFO	113.08	48.634	1.5209	135.00	27.000	203.20
Littlesyn-LIFO	118.56	49.891	1.5001	135.00	27.000	206.30
Littlesyn-SRPT	113.35	50.203	1.4908	135.00	27.000	195.00
Littlesyn-LRPT	123.52	43.870	1.5022	135.00	27.000	202.62
Littlesyn-EDD	117.47	49.243	1.5110	135.00	27.000	205.71

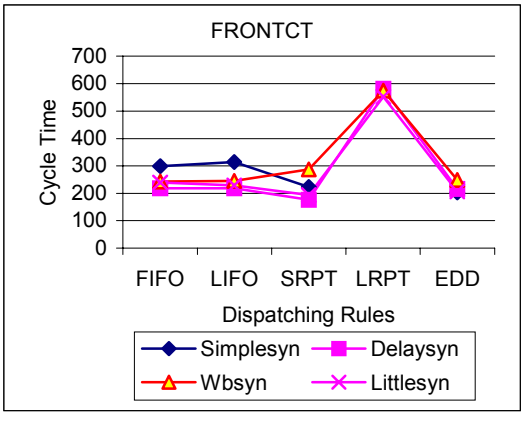

Figure 5: FRONTCT under Poisson Input Rule

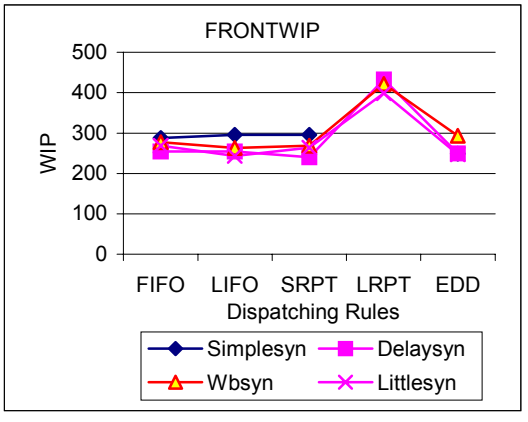

Figure 7: FRONTWIP under Poisson Input Rule

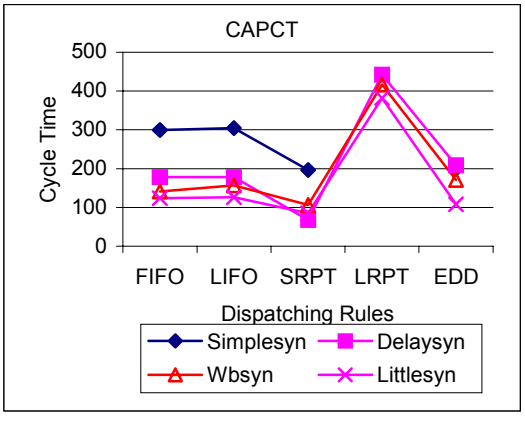

Figure 6: CAPCT under Poisson Input Rule

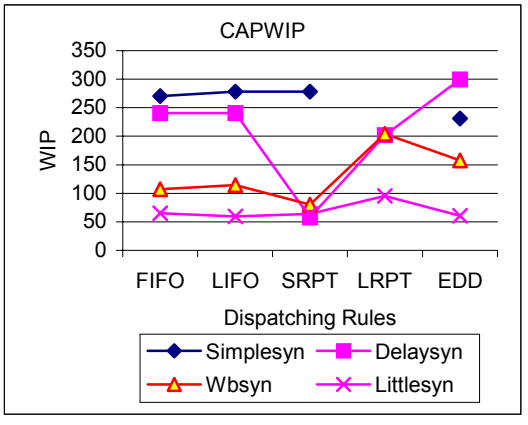

Figure 8: CAPWIP under Poisson Input Rule

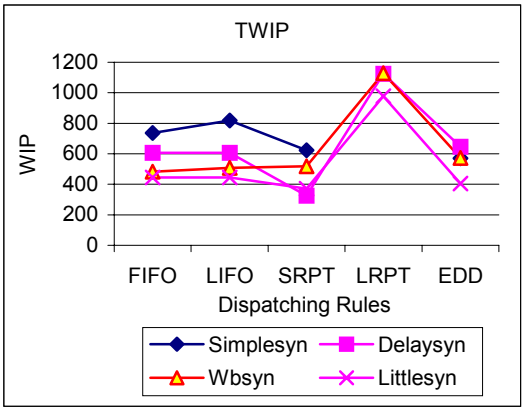

Figure 9: Total WIP under Poisson Input Rule

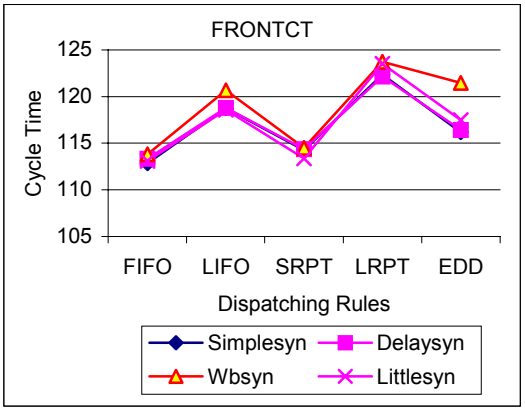

Figure 10: FRONTCT under CONWIP Input Rule

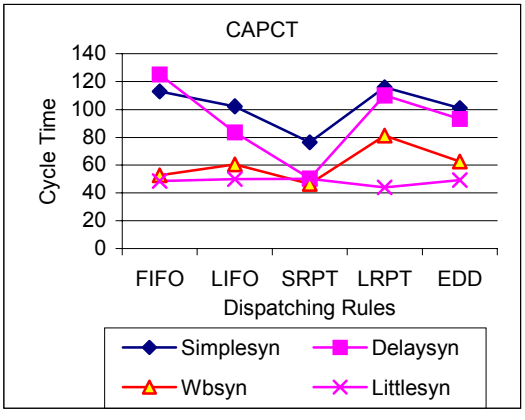

Figure 11: CAPCT under CONWIP Input Rule

confident intervals with a significance level of 0.05 (α=0.05) are listed. We only list the average values in table 2 because the corresponding confident intervals are very small under CONWIP release rule. Some data in Figures 5-9 are taken out because they are extremely large compared to the others. The figure with FRONTWIP under CONWIP input is not presented since it is a constant value.

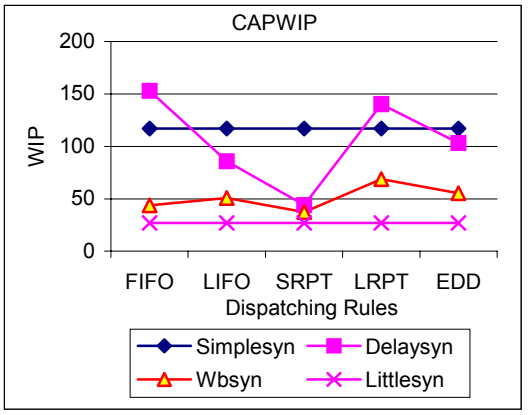

Figure 12: CAPWIP under CONWIP Input Rule

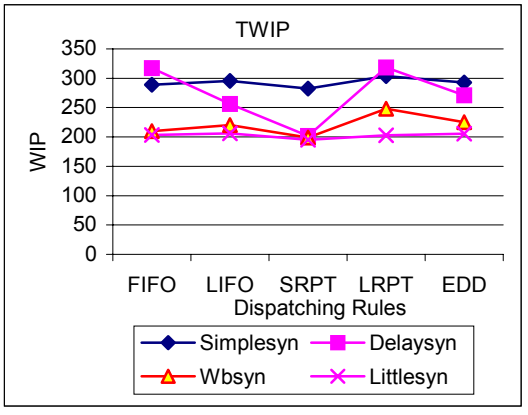

Figure 13: TWIP under CONWIP Input Rule

As can be seen from Figures 5, 6, 10, and 11 obviously, synchronization rules have significant impact on the performance of MEMS manufacturing. Both FRONTCT and CAPCT, especially CAPCT, change consistently under the four synchronization rules. Among the four synchronization rules, Littlesyn rule performs the best and gives the shortest cycle time. The reason is that Littlesyn rule is a closed-loop rule, which considers the relations on work-in-process between the front-end process and the cap process. Wbsyn rule results in the next shortest cycle time because it only focuses on the most heavily burdened workstations in the two sub-processes. Simplesyn rule and Delaysyn rule perform worse since they are open-loop rules. However Delaysyn rule is better because it considers the difference in the total processing time between the two sub-processes and deliberately releases the wafer later.

These four figures also indicate that the synchronization rules affect CAPCT more significantly than they do to FRONTCT. The reason is simple because the synchronization rules only control the raw wafer release in the cap process. However, an inefficient synchronization rule will also make FRONTCT long because the wafer in the front-end process might need to wait for the coming of the

wafer from the wafer cap process if the wafer cap process doesn't receive its release on time.

When comparing release rules for the wafer front end process, we find that CONWIP rule is much better than Poisson input rule by substantially reducing the mean value of cycle times and WIP levels as in results of previous research in semiconductor manufacturing. Those familiar with queuing theory will not be surprised by this, since the amount of variability in the processes is being reduced by switching from Poisson input to CONWIP input rule

It can be seen from figures 5, 6, 10, 11, that dispatching rules also have significant impact on the performance of MEMS manufacturing. Among the five dispatching rules, SRPT (shortest remaining processing time) rule gives the shortest cycle time. This is because SRPT rule gives priority to the earlier processed wafer and the wafer in the wafer cap process at the machines shared by both two sub-processes. So the cap wafer can arrive at the bonding workstation and meet the wafer output from the front-end process with less waiting time which leads to shorter cycle time. On the contrary, LRPT (longest remaining processing time) has the longest cycle time because it mainly gives priority to the later processed wafer and the wafer in the front-end process at the shared machine. Thus the wafer in the wafer cap process has to wait for a long time before it can meet the wafer from the wafer front-end process. As to the other dispatching rules, FIFO (first in first out), LIFO (last in first out), and EDD (earliest due date), they are worse than SRPT while better than LRPT because they do not intend to make the wafer in the wafer cap process move ahead faster.

In view of the simulation results, Littlesyn, CONWIP, and SRPT are the best in synchronization rules, lot release rules, and dispatching rules, respectively. However, we also need to find the best combination of these three scheduling rules. In this paper, we mainly consider about the cost of the wafers waiting in the process. For this reason, TWIP becomes the most important value because it includes the WIP in the wafer front-end process, the wafer cap process and the back end process. Therefore, unlike the other performance measures, FRONTCT, CAPCT, FRONTWIP, CAPWIP, which only involve relative information in one or two sub-processes, it represents the whole production line. Figures 9 and 13 show that Littlesyn-CONWIP-SRPT performs the best of these 40 combinations. Littlesyn-Wrsyn-SRPT and Littlesyn-Delaysyn-SRPT are the next best combinations.

It can be seen from the above figures that there is also a relatively high correlation between cycle time and WIP. This is as expected due to Little's Law. When the throughput rate is keep constant, cycle time and WIP level change at the similar way under different synchronization rules and dispatching rules. When cycle time is smaller, it shows that the waiting time in the production line is shorter. So the work-in-process in the production line is less, vice versa.

4 CONCLUSIONS

MEMS manufacturing is perhaps the most complicated manufacturing process. Discrete event simulation which is used in this problem, enables one to evaluate the process at a fraction of the cost and time actually needed for physical production. Although the assumptions do not strictly conform to the process, it is still the best alternative to evaluate the system.

We compare 40 combinations of four synchronization rules, two release rules and five dispatching rules in a MEMS production line. The results show that synchronization rules, release rules, and dispatching rules have significant impact on the performance of MEMS manufacturing. From the four synchronization rules studied, the Littlesyn rule gives the shortest cycle time, which means it coordinates the best between the release of the front-end process and the wafer cap process. As to the release rule and dispatching rule, CONWIP and SRPT are recommended respectively. And the best rules combination is the Conwipsyn-CONWIP-SRPT policy.

In this paper, although we only consider simple synchronization rules, release rules, and dispatching rules for MEMS manufacturing, it provides a good framework for developing more sophisticated scheduling rules. In addition, more complicated input mechanisms to be used in the front-end process, e.g. starvation avoidance, workload regulating, should be also considered. Besides, more general MEMS production lines, such as those with multiple types of products, including machines failure and maintenance, are necessary to be studied in future.

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