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# A SIMULATION STUDY ON RELEASE, SYNCHRONIZATION, AND DISPATCHING IN MEMS FABRICATION

Lixin Wang

Gintic Institute of Manufacturing Technology
71 Nanyang Drive
638075, SINGAPORE

Loo Hay Lee

Department of Industrial & Systems Engineering
National University of Singapore
10 Kent Ridge Crescent
119260, SINGAPORE

## ABSTRACT

MEMS (microelectromechanical system) fabrication can be organized as three sub-processes, that is, the front-end process, the wafer cap process, and the back-end process. The coordination between the releases of raw wafers to the two parallel sub-processes, the front-end process, and the wafer cap process, is always an important issue. Previous research work has developed synchronization rules to create effective coordination. In this paper, new synchronization rules and dispatching rules are developed and they are evaluated with more release rules. From this much more extensive simulation experiment, it is found that there are significant two-factor and three-factor interactions among these three types of rules and we have to consider them all together in order to achieve the best performance for MEMS fabrication system. Moreover, the complicated relationship between the performances (cycle time and total work-in-process) is also indicated.

## 1 INTRODUCTION

MEMS (Micro-Electromechanical Systems) are integrated micro devices or systems combining electrical and mechanical components fabricated using integrated circuit (I-C) compatible batch-processing techniques. They range in sizes from micrometers up to a couple of millimetres. These systems can sense, control, and actuate on the micro scale and function individually or in arrays to generate effects on the macro scale. Current MEMS applications include accelerometers, pressure, chemical and flow sensors, micro-optics, optical scanners and fluid pumps.

The MEMS fabrication process studied in this paper is based on a commercial SCREAM (single crystal reactive etching and metallization) micromachining technology. This technology uses reactive ion etching both to define and release structures (Madou 1997). The production process can be organized as three sub-processes, namely, the front-end process, the wafer cap process, and the back-end process (see Figure 1). Raw wafers are initially released to the two parallel sub-processes, the front-end process, and the wafer cap process, with a batch size of eighteen wafers. Then they are processed in these two sub-processes with this batch size concurrently. Every wafer that has undergone all the operations in the front-end process will be bonded with a wafer which has completed all the operations in the wafer cap process at the bonding machine. The bonded wafer then continues its processing in the back-end process individually.

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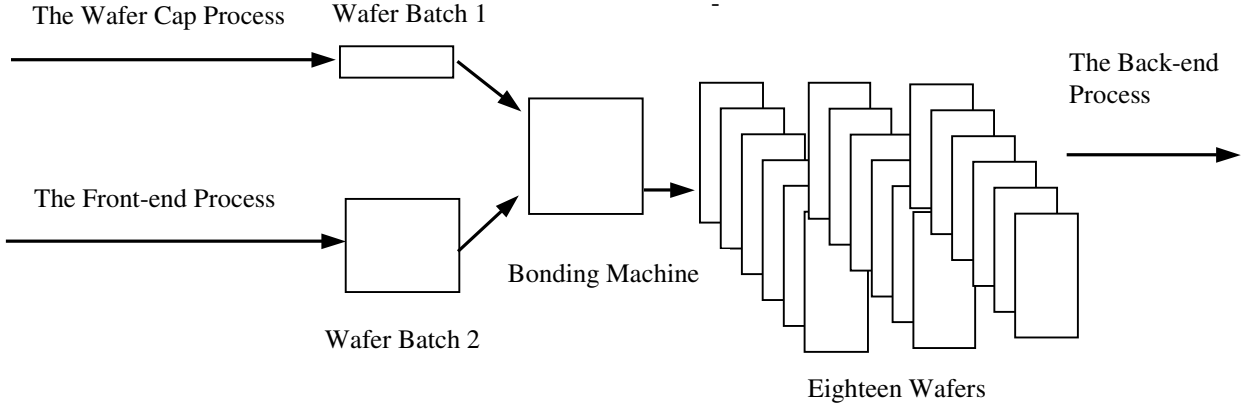


Figure 1: Schematic View of the Whole MEMS Process

MEMS fabrication processes combine IC and micro-machining processes. Consequently, the process flows and the equipment used in MEMS fabrication are very similar to those for semiconductor manufacturing. As pointed out by Johri (1993) and Duenyas, Fowler, and Schruben (1994), semiconductor manufacturing is one of the world's most complicated manufacturing processes. Scheduling in semiconductor manufacturing is always a very tough issue. There have been a lot of studies in this area (Glassey and Resende 1988a and 1988b, Wein 1988, Lawton et al. 1990, Spearman, Woodruff, and Hopp 1990, Kim et al. 1998). Uzsoy, Lee, and Martin (1992, 1994) have also provided extensive surveys on production scheduling in the wafer industry. These studies showed that production scheduling could significantly improve the performance measures of wafer fabrication. In addition, Fowler, Cochran, and Horng (1999) presented a study of the published literature in modelling and simulation of semiconductor manufacturing operations that they used to build a searchable database which was implemented as an Internet site. Due to the similarities between MEMS manufacturing and wafer fabrication, some of these production scheduling rules and research methods can also be applied in MEMS.

However, the MEMS process is also not exactly same as wafer fab process, and it has its special characteristics which make the scheduling problems even more challenging. The wafer cap process usually takes a smaller number of steps and amount of time to complete the process than the front-end process, and so one of the critical issues is the coordination of the release of these two sub-processes such that wafers from them could arrive at the bonding workstation about the same time. Besides, there are several workstations which are shared by both the front-end process and the wafer cap process. If this synchronization problem is not properly managed, there will be an unnecessary increase in the cycle time of the products (the time from the release of the raw material to the final product) and the WIP level.

Since MEMS is a newly developed technology, very few studies have been carried out directly on production scheduling in MEMS fabrication. As for the synchronization problem in MEMS fabrication, this is exactly a new research area. Previously, Wang, Tay, and Lee (2000) developed four synchronization rules and they are evaluated together with two release rules and five dispatching rules. The simulation results indicated that all these three types of rules have significant impacts on the performance of MEMS manufacturing. However, this paper has not done extensive analysis on the interactions among the three types of rules and it did not explore the relationship between the performances. Therefore, further research work needs to be done in MEMS scheduling

In this paper, five synchronization rules are introduced to coordinate the releases of the front-end process and the wafer cap process. These rules are used together with five release rules and six dispatching rules to evaluate the performance of the MEMS fabrication system. Since the MEMS process is very complicated, a discrete event simulation model is built to imitate its process flows.

The remainder of this paper is organized as follows. Section 2 describes three types of rules for production scheduling and the simulation experiments are provided in Section 3. In Section 4, the results of the simulation study are presented and discussed, and the conclusions of the study are contained in Section 5.

## 2 RULES FOR PRODUCTION SCHEDULING

Owing to its complexity, three types of rules are considered for production scheduling and control in this MEMS manufacturing system (see Figure 2). They are release rules (also known as input rules), synchronization rules, and dispatching rules. Release rules dictate the release of raw wafers to the process. Synchronization rules are new rules developed in this paper to release raw wafers to the process in coordination with release rules. Since the front-end process is the main part of the whole MEMS process and it takes longer time to complete the process, it will be more manageable and simpler to apply synchronization rules to control the release mechanism of the wafer cap process. Therefore, the authors use release rules to decide when to release raw wafer batches into the front-end process. After one wafer batch has been released into the front-end process, the release of a raw wafer batch to the wafer cap process is determined by synchronization rules. Dispatching rules are used to decide which wafer or wafer batch waiting at a workstation is to be processed first when the workstation is free.

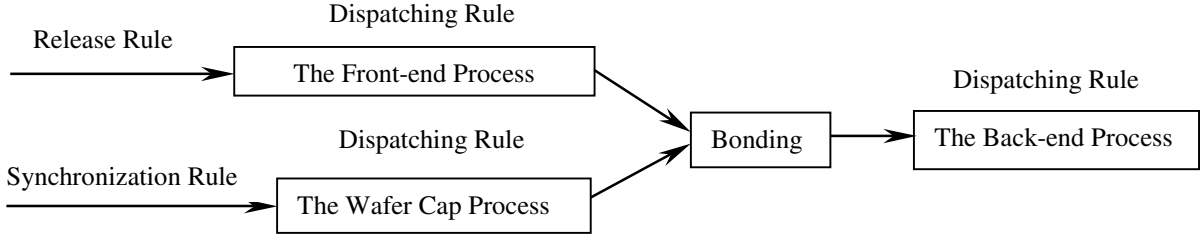


Figure 2: Schematic of the MEMS Fabrication Process with Three Types of Rules

### 2.1 Release Rules

Under release rules, a new wafer batch is released into the front-end process when certain conditions are satisfied. In this paper, five release rules are used. They are described in Table 1.

Table 1: Descriptions of Release Rules

| | |
|---|---|
| POIS -SON | The inter-arrival times of the order release follow an exponential distribution |
| UNIF | New wafer batches are released into the process at a constant rate |
| CON-WIP | A new wafer batch is released whenever a batch has completed all the operations (Spearman, Woodruff, and Hopp 1990) |
| SA | A new wafer batch is released when virtual inventory at the bottleneck workstation falls below a predetermined value (Glassey and Resende 1988a and 1988b) |
| WR | A new wafer batch is released when the workload at the bottleneck workstation falls below a critical value (Wein 1988, Lawton et al. 1990) |

### 2.2 Synchronization Rules

Synchronization rules control the release of a raw wafer batch to the wafer cap process after a new batch has been released to the front -end process. Under synchronization rules, a new wafer batch will be released into the wafer cap process when certain conditions are satisfied. Usually the conditions include certain information from both the front-end process and the wafer cap process. This means synchronization rules are not independent of release rules. Their descriptions are as follows:

**SIMPLESYN** (simple synchronization)**.** A wafer batch will be released into the wafer cap process at the same time as a batch is released to the front-end process.

**DELAYSYN** (delayed-release synchronization). This rule is to delay the release of the wafer cap process by a constant time $\Delta T$, which is defined as the difference between the sum of the processing time of the front-end process and the wafer cap process.

**WBSYN** (workload balancing synchronization). It focuses on the workload at the bottleneck machine (Wein 1988, Lawton et al. 1990). In this rule, raw wafers are released to the wafer cap process to balance the workload between the two most utilized machines in these two subprocesses. As described previously, the MEMS production line is too complicated to be analyzed intuitively (see Figure 3). Therefore, the whole production line is first simplified to a virtual flow shop which is shown in Figure 4. Then bottleneck machines of both the front-end and wafer cap process are identified, which are denoted by machine *A* and *B*. A procedure for applying the WBSYN rule is given below.

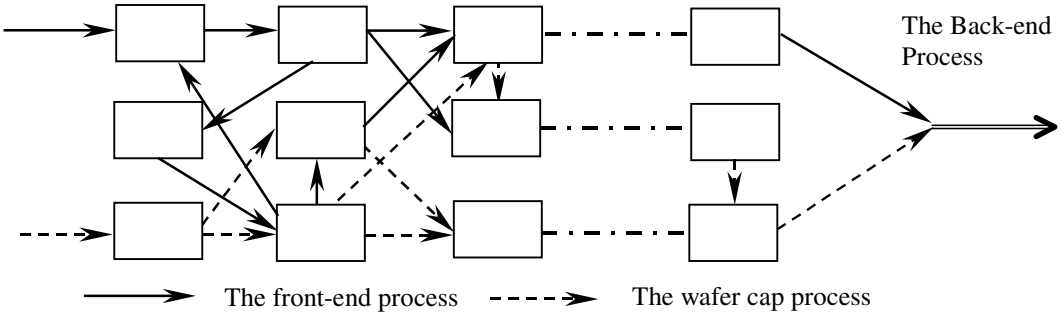


Figure 3: Schematic Representation of the Front-end Process and the Wafer Cap Process

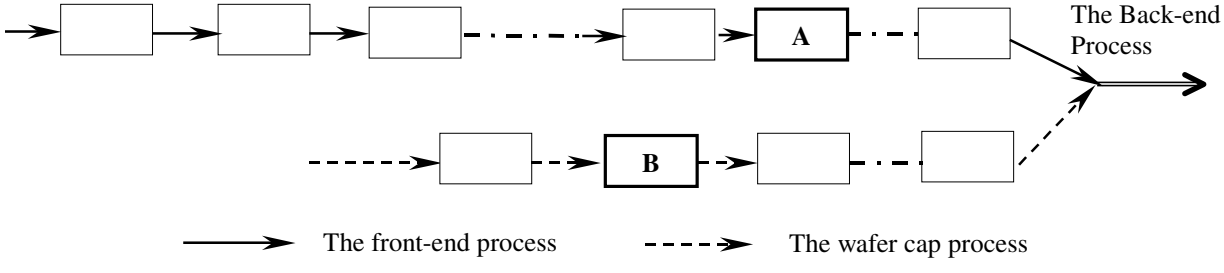


Figure 4: Schematic Representation of WBSYN Rule with the Virtual Flow of the Front-end and the Wafer Cap Process

*Procedure (WBYSN)*
*Step 1*. Calculate WIP inventory of bottleneck machine A and B ($WIP_A$ *and* $WIP_B$)
*Step 2*. If $WIP_A > WIP_B$, then release one wafer batch to the wafer cap process, else do not release.
*Step 3*. Go back to step 1.

**LINESYN** (line balancing synchronization). The idea for this rule is to balance the WIP for the front-end process and the wafer cap process. Since the total processing time for these two sub-processes are different, the ideal WIP level for these two processes should also be different. A simple approximation would be the ratio of the WIP of the two sub-processes should be equal to the ratio of the total processing time in the two sub-processes.

Let $WIP_1$ *and* $WIP_2$ be the mean number of waiting wafers in the front-end and wafer cap process respectively. Similarly, let $T_1$ and $T_2$ denote the total processing time for these two sub-processes. A procedure for applying the LINESYN rule is given below.

*Procedure (LINESYN)*
*Step 1*. Calculate WIP inventory ($WIP_1$*and* $WIP_2$)
*Step 2*. If $WIP_1 > WIP_2 \times (T_1 / T_2)$, then release one wafer batch to the wafer cap process, else do not release.
*Step 3*. Go back to step 1.

**SASYN** (starvation avoidance synchronization). This rule is adopted from the starvation avoidance input rule for wafer fabrication (Glassey and Resende 1988a and 1988b). The idea is to treat the bonding station as the bottleneck machine. The raw wafers will be released to the wafer cap process so as to avoid the idling of the bonding machine. Let $WIP_{P1}$ be the total WIP in the last portion of the front-end process with a total processing time roughly equal to the total processing time of the wafer cap process (see Figure 5). $WIP_2$ is the total WIP in the wafer cap process. Similar to the SA rule, the virtual inventory at the bottleneck (the bonding station) in the front-end process is denoted as $WIP_{P1}$ and the virtual inventory of the wafer cap process is denoted as $WIP_2$. A procedure for applying the SASYN rule is given below.

*Procedure (SASYN)*
*Step 1*. Calculate WIP inventory ($WIP_{P1}$ *and* $WIP_2$)
*Step 2*. If $WIP_{P1} > WIP_2$, then release one wafer batch to the wafer cap process, else do not release.
*Step 3*. Go back to step 1.

### 2.3 Dispatching Rules

The First In First Out (FIFO) dispatching rule and Shortest Remaining Processing Time (SRPT) rule are used in this study because they are widely used in practice. In addition, the author developed another four rules, namely, CAPFIFO, FRONTFIFO, CAPSRPT, and FRONTSRPT by giving processing priority to the wafers in the front-end process or those in the wafer cap process at the workstations shared by these two sub-processes. E.g., in CAPFIFO rule, FIFO is utilized for all the workstations except the workstations shared by both the front-end and wafer cap process in which case priority is given to the wafer batches in the wafer cap process. Totally, six dispatching rules are studied.

## 3 SIMULATION EXPERIMENTS

To compare all the rules introduced in this study, a series of simulation experiments is performed. Performance measures used for the comparison are the cycle time of the wafer, i.e., the time between the release of the raw wafer to the front-end process until it comes out from the back-end process (CT), and total work-in process in the whole process (TWIP).

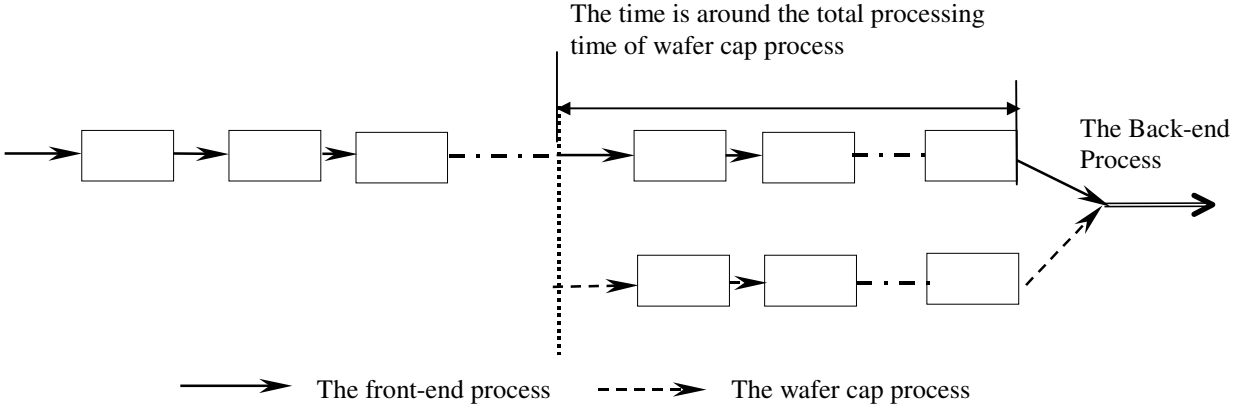


Figure 5: Schematic Representation of SASYN Rule with the Virtual Flow of the Front-end and the Wafer Cap Process

The MEMS production line considered in this study consists of 106 steps in the front-end process, 24 steps in the wafer cap process, and 18 steps in the back-end process. It consists of 37 single-server or multiserver workstations, and all multiserver stations consist of identical equipment. The bottleneck workstation is the dry etch workstation in the front-end process. A wafer in the front-end process has to visit this workstation 5 times. We consider only a single MEMS product to be produced in the production line.

Processing time for a wafer at one station is randomly generated from a uniform distribution between 0.9×MPT and 1.1×MPT, where MPT is the mean processing time for each station. The simulation model includes random machine breakdowns and scheduled maintenance. Time between failures and time to repair for each workstation are randomly generated from exponential distributions with the given mean time between failure (MTBF) and mean time to repair (MTTR). The transfer time between workstations is negligible because it is much smaller than the processing time and the machine downtime.

In this study, five synchronization rules, five release rules and six dispatching rules which resulted in 150 (5×5×6) combinations are investigated. The release rate under POISSON input and UNIF input is 0.0775 batch/hour, or 1.3950 wafers/hour. With this release rate, the percent utilization is around 92% for the single bottleneck station. The CONWIP, WR and SA input rules are adjusted so that the utilization of the bottleneck machine is also around 92%. It should be noted here that in this paper, we are trying to optimize the performance (CT and TWIP) given that output maintained at a given level. This is true in practice especially because output is always driven by demand, and output can be achieved by how fast your release to the line (on the condition that the system is stable).

A significant part of any simulation study is the verification and validation (V&V) of the simulation model. Verification is the process of ensuring that the model design (conceptual model) is transformed into a computer model with sufficient accuracy, in other words, building the model right. The simulation software used provides some methods in model verification, e.g., animation function, which shows the flow of items in a model, levels of values and so forth. More details on verification and validation of this MEMS manufacturing model can be found in Lixin (2001).

In the simulation experiments, each rule combination underwent 20 replications (runs) and each simulation run was carried out for a simulation time of 25,000 hours. Different random seeds were used for the 20 runs, and each run was started with an empty line. To obtain system performance in a steady state, statistics of the initial transient period (1,5000 hours) of each run were excluded from analysis. The results indicate that the standard deviation of the average performance found is within 10 percentage of the corresponding mean value. The simulation models were built using *EXTEND (version 4.01),* a simulation software developed by Imagine That Inc. and the simulation tests were carried out on a personal computer with a Pentium II (500 MHz) processor.

## 4 SIMULATION RESULTS AND DISCUSSIONS

### 4.1 Simulation Results for CT

Simulation results for cycle time CT of the 150 combinations are given in Figures 6-10. To show the effects of the rules and identify the differences in the performance, an analysis of the variance (ANOVA) using Minitab was carried out and the results are shown in Table 2. The analysis results show that all these three types of rules (release rules, synchronization rules, and dispatching rules), have significant effects on the cycle time for the MEMS manu-

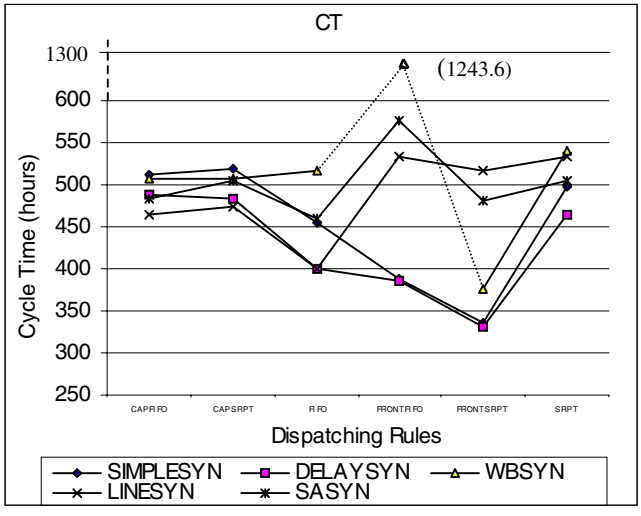


Figure 6: CT under POISSON Input Rule

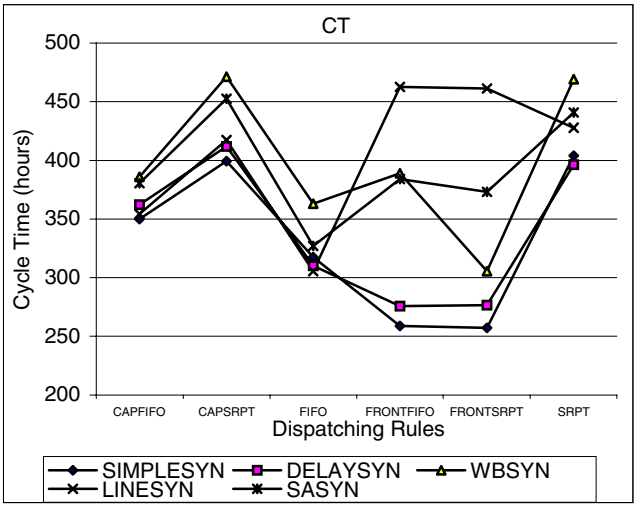


Figure 7: CT under UNIF Input Rule

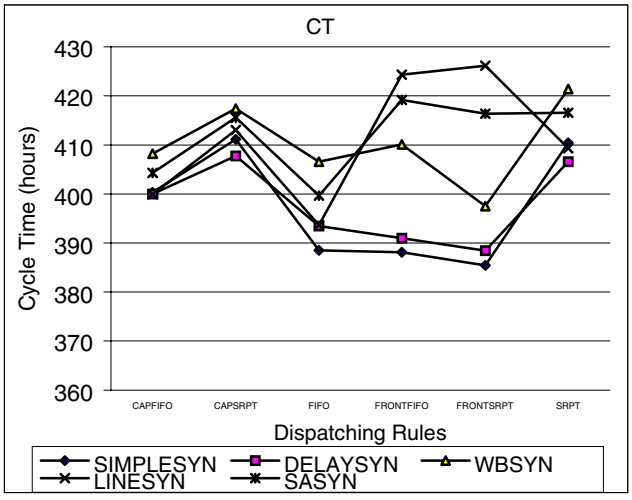


Figure 8: CT under CONWIP Input Rule

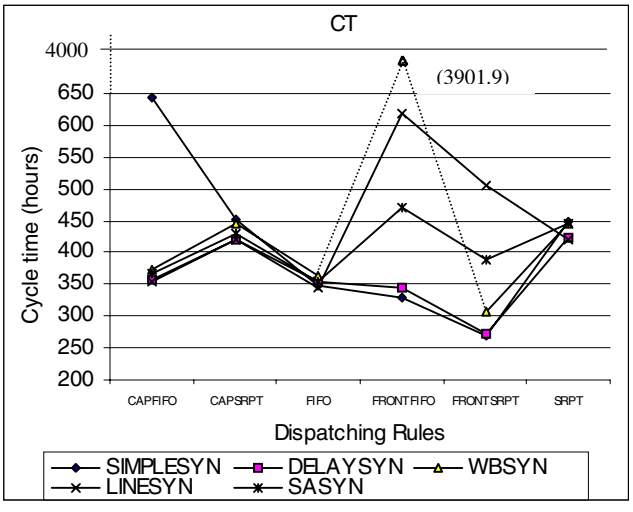


Figure 9: CT under SA Input Rule

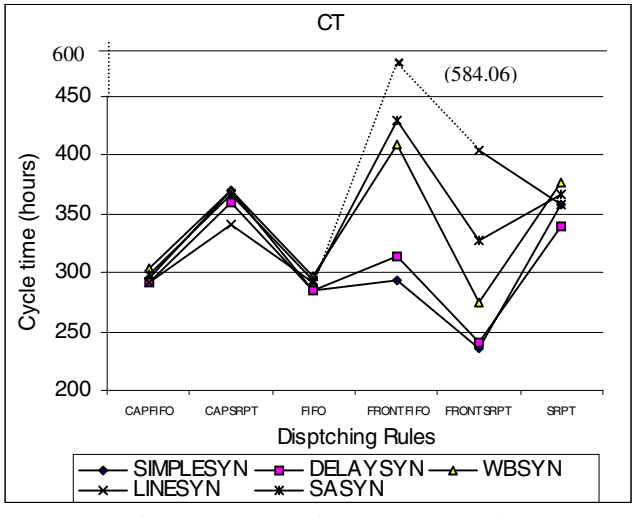


Figure 10: CT under WR Input Rule

Table 2: Analysis of Variance of CT

| Source of Variation | F | P |
|---|---|---|
| Release | 174.58 | <0.001 |
| Synchronization | 141.15 | <0.001 |
| Dispatching | 160.44 | <0.001 |
| Release×Synchronization | 64.38 | <0.001 |
| Release×Dispatching | 76.30 | <0.001 |
| Synchronization×Dispatching | 118.52 | <0.001 |
| Release×Synchronization×Dispatching | 70.27 | <0.001 |

facturing system and there are also significant two-factor and three-factor interactions among these rules.

Since the wafer which completes the front-end process needs to be bonded with the wafer from the wafer cap process, it will not be hard to see why the synchronization rules which control the release of the wafer cap process will have significant effects on CT. Among the five synchronization rules, open-loop rules (SIMPLESYN and DELAYSYN) perform better than closed-loop rules (SASYN, LINESYN, and WBSYN). Under the SIMPLESYN and DELAYSYN rule, wafers in the wafer cap process will always arrive at the bonding workstation earlier than those in the front-end process because wafers from wafer cap process spend shorter time in waiting and completing its process. Therefore, the bonding operation can be started immediately once a wafer has completed its front-end process, and hence small cycle time will be expected. On the other hand, SASYN, LINESYN, and WBSYN rules attempt to coordinate the release between these two sub-processes, but they cannot guarantee the arrival of the wafers from wafer cap process can be earlier than those from the front-end process. As a result, a longer cycle time will be incurred.

As can be seen from the figures above, there are also significant differences in CT under different release rules and dispatching rules. Among the five release rules, WR performs the best which is also consistent to the research results (Wein 1988) in the semiconductor manufacturing. As for dispatching rule, the analysis results using Minitab show FRONTSRPT performs the best and then followed by FIFO and FRONTFIFO rule performs the worst.

From the analysis, we could also observe that there are significant two-factor and three-factor interactions between the rules. For example, there is a significant interaction between the synchronization and dispatching rules. The analysis results show that under SIMPLESYN and DELAYSYN rules, FRONTSRPT yields the best performance while under LINESYN and SASYN rules, the performance of FRONTSRPT is not good. The reason is that under SIMPLESYN and DELAYSYN, wafers in the wafer cap process arrive at the bonding station earlier than those in the front-end process and FRONTSRPT which gives priority to the wafers in the front-end process

will make them move ahead faster, and hence help reduce the cycle time. As a result, it will be important to consider all the rules together so that all their interactions can be captured.

Among the 150 combinations of the rules, we have listed the rule combinations that have the best performance in Table 3. Due to the stochastic nature of the results, Fisher's Least Significance Difference (LSD) Pairwise comparisons tests (at the significant level of 0.01) are carried out in order to identify those rule combinations which don't have significant differences with the best rule combination.

Table 3: the Best Rule Combinations for CT

| Rule Combination |
|---|
| WR-SIMPLESYN-FRONTSRPT |
| WR-DELAYSYN-FRONTSRPT |

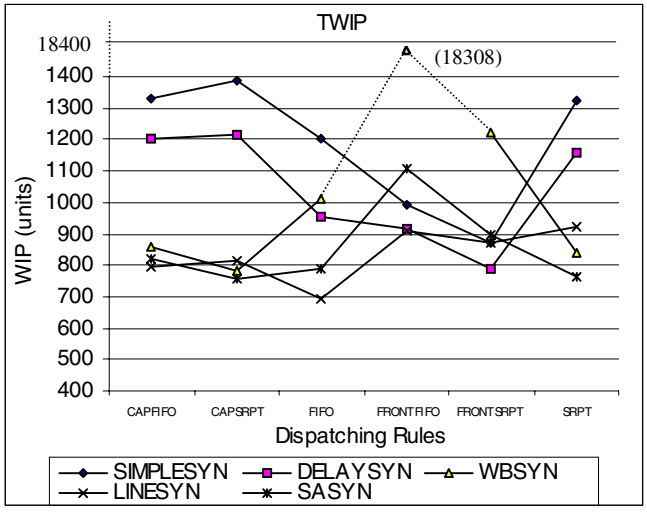


Figure 11: TWIP under POISSON Input Rule

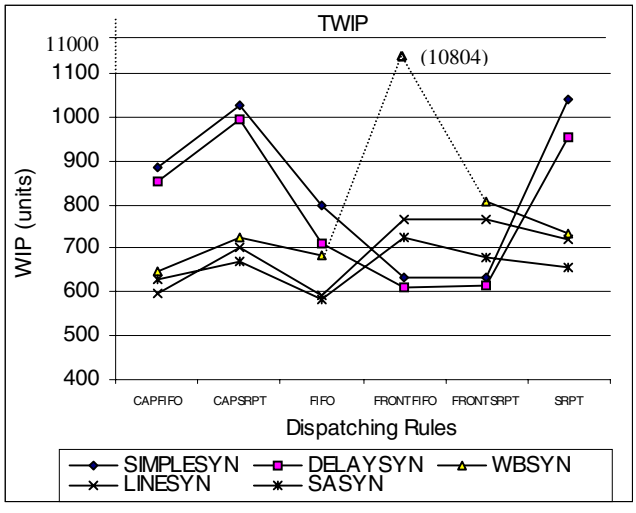


Figure 12: TWIP under UNIF Input Rule

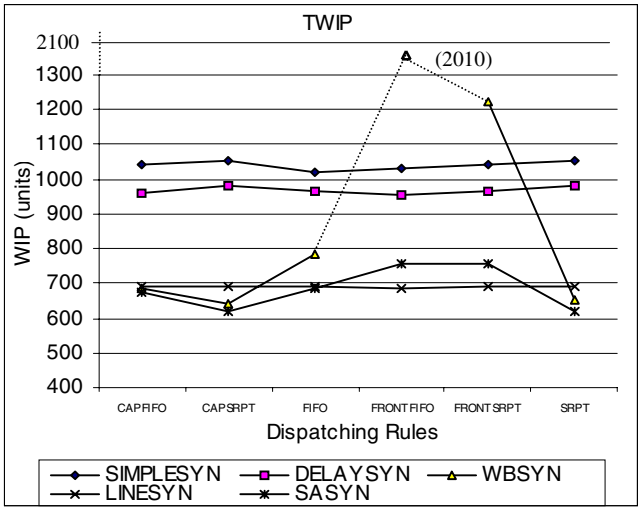


Figure 13: TWIP under CONWIP Input Rule

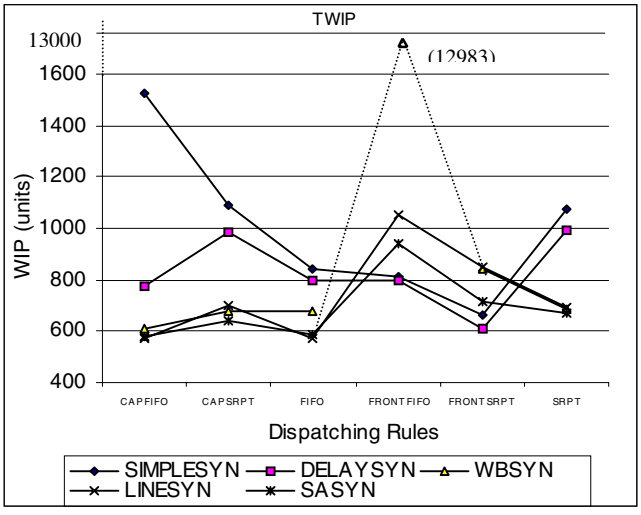


Figure 14: TWIP under SA Input Rule

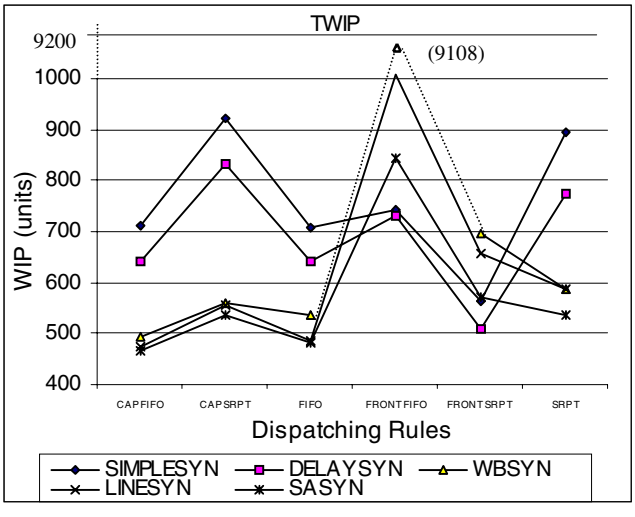


Figure 15: TWIP under WR Input Rule

Table 4: Analysis of Variance of TWIP

| Source of Variation | F | P |
|---|---|---|
| Release | 126.83 | <0.001 |
| Synchronization | 504.17 | <0.001 |
| Dispatching | 546.96 | <0.001 |
| Release×Synchronization | 113.16 | <0.001 |
| Release×Dispatching | 114.34 | <0.001 |
| Synchronization×Dispatching | 529.46 | <0.001 |
| Release×Synchronization×Dispatching | 112.62 | <0.001 |

### 4.2 Simulation Results for TWIP

The results for TWIP are given in Figures 11-15. The results of ANOVA are shown in Table 4. Similarly to CT, according to the ANOVA results, the release, synchronization, and dispatching rule have significant effects on the total WIP for the MEMS manufacturing system.

However, different from the results of CT, the analysis shows that the best synchronization rule for TWIP is SASYN and LINESYN. The reason is because these two rules tempt to coordinate the releases of the front-end and the wafer cap process, which help to reduce unnecessary WIP at the wafer cap process. As for the dispatching rule and release rules, the results are quite similar to the results for CT.

Similar to CT, there are also significant interactions between rules, for instance, under SIMPLESYN and DELAYSYN, FRONTSRPT yields the best performance but under LINESYN and SASYN, it is one of the worst rules. As a result, to find the best rule, we need to consider all the 150 rule combinations together. According to the LSD comparisons tests (at the significant level of 0.01), the best rule combinations for the TWIP is listed in Table 5.

Table 5: the Best Rule Combinations for TWIP

| Rule Combination |
|---|
| WR-SASYN-CAPFIFO |
| WR-LINESYN-CAPFIFO |

### 4.3 CT vs. TWIP

From Tables 3 and 5, it can be seen that the best rule combinations for the two performance measures are different. However, both the CT and TWIP are important indicators for the performances of the systems. A scatter plot for CT and TWIP for the 150 rule combinations is shown in Figure 16. From the figure, it can be seen that the shortest CT and smallest TWIP can not be achieved at the same time. In fact, this is a multi-criteria optimization problem. To find an efficient solution for this problem, we have to find the efficient frontier for the solution. In Figure 16, those solutions which are located at the left hand corner will be the efficient solution. There are four rule combinations which are located at the efficient frontier, and they are listed at Table 6. Since there is no rule combination among these four can dominate others both in term of CT and TWIP, and they will be considered equally good. One can select the rule combinations according to his detailed requirements and conditions. For example, if cycle time is the most concerned or the cost of WIP inventory is small compared to other costs, one would like to use the best rule combinations for CT at the expense of a larger TWIP, (e.g. WR-SIMPLESYN-FRONTSRPT or WR-DELAYSYN-FRONTSRPT). However if the cost of WIP inventory is very high, then the best rule combination for TWIP will be a better choice, for example, WR-SASYN-CAPFIFO and WR-LINESYN-CAPFIFO.

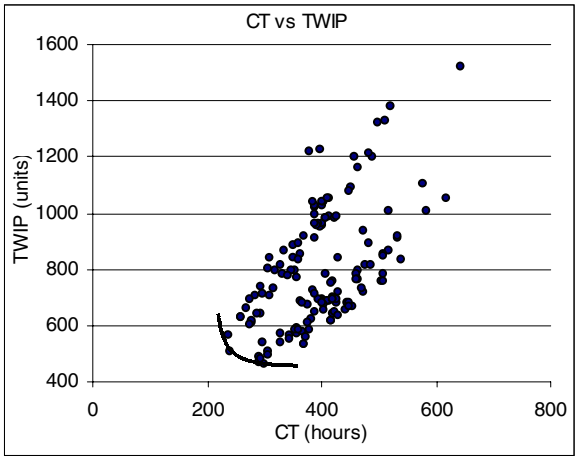


Figure 16: Results of the 150 Rule Combinations for CT and TWIP

Table 6: the Best Efficient Rule Combinations for Both CT and TWIP

| Rule Combinations | CT (hours) | TWIP (units) |
|---|---|---|
| WR-SIMPLESYN-FRONTSRPT | 236.56±2.69 | 564.87±5.01 |
| WR-DELAYSYN-FRONTSRPT | 240.08±2.47 | 507.60±5.41 |
| WR-LINESYN-CAPFIFO | 291.26±2.00 | 473.25±2.17 |
| WR-SASYN-CAPFIFO | 298.74±1.51 | 467.21±2.75 |

## 5 CONCLUSION

MEMS fabrication is one of the most complex manufacturing processes in the world. It has its special characteristic which is different from normal semiconductor manufacturing. In this paper, the authors develop five synchronization rules to coordinate the releases of the wafers into the front-end process and the wafer cap process. They are evaluated together with five release rules and six dispatching rules re-

sulting in a total of 150 rule combinations. The simulation results show that all three types of rules can have significant impact on the performance of MEMS fabrication. Moreover, there are significant two-factor and three-factor interactions among these rules. The best rule combinations for the two performances measures, CT and TWIP, are also identified.

In this paper, although the authors only considered simple synchronization, release, and dispatching rules for MEMS fabrication, it provides a good framework for developing more sophisticated scheduling and control rules. First, other sophisticated synchronization rules, especially those based on mathematical models, such as queueing network models, can be developed to improve the performance measures. In addition, unlike the commonly used rules (FIFO and SRPT), new dispatching rules, e.g., those focusing on the dispatching sequences of wafers waiting at the machines shared by both the front-end and wafer cap process, can be specifically developed for the MEMS production line to improve performance measures. Besides, a more general MEMS production line with multiple types of products has to be studied in future.

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## AUTHOR BIOGRAPHIES


**LIXIN WANG** is currently an associate research fellow at Gintic Institute of Manufacturing Technology, Singapore. He got a bachelor degree in the Department of Precision Instruments and Mechanology from Tsinghua University, Beijing China in 1997. Later, he obtained his Master degree from the Department of Mechanical Engineering, National University of Singapore in 2001. His research area is Production Planning and Scheduling in MEMS Manufacturing and Semiconductor Manufacturing. He is also a member of IEEE and APICS. His email address is <lxwang@gintic.gov.sg>.

**LOO HAY LEE** is an assistant professor in the Department of Industrial and Systems Engineering at the National University of Singapore, Singapore. He obtained his B.S. in Electrical Engineering from National Taiwan University in 1992. Subsequently, he received a M.S. degree in Engineering Science from Harvard University in 1994 and a Ph.D. degree from the same university in 1997. His research interests include Discrete Event Dynamic Systems, Ordinal Optimization, Systems Modeling and Simulation, and Decision & Control. He is also a member of IEEE and INFORMS. His email is <iseleelh@nus.edu.sg>.