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SIMULATION ANALYSIS OF THE CONTROL POINT POLICY FOR SEMICONDUCTOR FAB LINES PRODUCING MULTIPLE PART TYPES

Talha Liaqat
Young Jae Jang

Department of Industrial and Systems Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon, 305-701, REPUBLIC OF KOREA

ABSTRACT

In this paper, we introduce a new modified version of the scheduling approach, Control Point Policy (CPP) for semiconductor wafer fabrication lines and compare its performance with the popular Earliest Due Date (EDD), Minimum Slack (MS) and Critical Ratio (CR) scheduling policies. Discrete event modeling and simulations are created to evaluate the performance of CPP for three important performance measures; *cycle times*, *waiting times* and *inventory levels*. New insights for system performance are developed with the implementation of CPP at bottleneck stations and the introduction of finite size buffers between all the workstations. Our simulation results demonstrate the ability of CPP to achieve lowest cycle times with minimum inventory levels for situations where products with similar process characteristics are prioritized over each other. Our simulation experiments show that the CPP generates good system performance for environments where multiple products at different processing stages compete for limited resources.

1 INTRODUCTION

Modern semiconductor fabrication lines are considered the most complex and dynamic class of manufacturing systems. In recent scenarios of high market competition coupled with increasing customer demands and varied product characterizations, companies are focusing on improving their manufacturing operations to achieve lower cycle times and maintaining minimal inventory levels. Semiconductor manufacturing comprises of four processes namely: wafer fabrication, wafer probe, wafer packaging and final testing of the wafers produced. The wafer fabrication process involves photolithography, etching, thin film, ion implantation and diffusion. We considered the operations involved in wafer fabrication (fab) for our research, since it is the most technologically complex and comprises the major capital investment for semiconductor fabrication lines.

The semiconductor fab is often characterized by the repetitive use of several similar processing operations. The machines performing these operations are very expensive especially the photolithography machines. Therefore, the selection of appropriate scheduling policies is critical for the performance of highly congested semiconductor fab lines.

Generally, scheduling policies are characterized as *parts release* and *lot sequencing rules*. In this paper, we introduce a new scheduling policy, known as Control Point Policy (CPP). The CPP, being a combination of both parts release and lots sequencing rules maintains inventory levels as per operating demands, while minimizing the earliness and tardiness penalties for the lots reaching the finished goods buffers. The CPP is useful for scenarios where the companies maintain different priorities for products with similar due dates and other process characteristics. Another characteristic of the CPP is its performance for multiple products assembly lines with finite size buffers, and comprising of highly re-entrant flows leading to disorderly intermingling of parts at several workstations. Since the semiconductor fab lines involves the simultaneous

production of different prioritized products competing for limited resources, the CPP is expected to give a better system performance in comparison to other policies.

The goal of the research is to analyze the performance of the CPP for semiconductor fab lines for three important performance measures; *cycle times*, *waiting times*, and *work in process* levels. The performance of the CPP is compared with other make-to-order rules such as Earliest Due Date (EDD), Minimum Slack (MS) and Critical Ratio (CR). In our analysis we focus on the due-date based scheduling of the fab operation since most foundary semiconductor fabs operate with a make-to-order production with promised due-date for the order. Also some memory chip makers including Samsung Electronics and Micron Technology specify the due-date in each lot to manage the cycle time. In our study, simulations are developed for a semiconductor fab line capable of processing multiple parts with different priorities and demands. Finite size buffers are introduced between workstations to observe the phenomena of machines starvation and blockage, and to reflect a situation more closer to the actual fab operations. The CPP is implemented at multiple work stations including the bottleneck stations and the improvement in system performance is measured. This paper also provide insights for the future developmental work of the CPP.

Section 2 introduces a brief description of the policies, previous work done with CPP, and the improvements made in the policy with this research. Section 3 gives a detailed description of time based version of CPP and its modeling in our simulation. Section 4 describes the simulation model developed for our research. Section 5 discusses the results of the simulation experiments. Section 6 summarizes the approaches and findings and discusses the future research.

2 LITERATURE REVIEW

Scheduling policies for semiconductor manufacturing can be classified for two categories; set of rules designed for *make-to-stock* and *make-to-order* systems. Most commonly used make-to-stock rules include CONWIP (Spearman, Woodruff, and Hopp 1990), BASE STOCK (Kimball 1988), and KANBAN (Berkley 1992). Earliest Due Date(EDD), Minimum Slack(MS), and Critical Ratio(CR) are the most commonly employed rules for make-to-order semiconductor manufacturing environments. The EDD rule push the products on the basis of due dates regardless of the penalties for backlog, surplus and without differentiating the valuable products from the others. Least slack policy considers the performance of the part as per its schedule. However, it does not distinguish the parts that are earlier than their slack times, and sometimes result in unnecessary flooding of parts in the downstream buffers. The CR policy is the most widely used policy in multi-parts, make-to-order manufacturing environments. It evaluates the parts on the basis of their remaining expected processing times and their due dates. Those parts getting late are given a priority over the non-late parts. However, the policy assigns same priority to parts with similar critical ratio values, without distinguishing about the part type. The policy also requires whole set of computations to be performed in the upstream buffers each time a part completes its processing on the machines.

Gershwin (2000) first introduced control point policy (CPP) for multiple parts, multiple process re-entrant manufacturing systems. Gzouli (2000) implemented the policy for single-part types in make-to-stock systems and showed its superior characteristics as compared to *KANBAN*, *CONWIP* and *BASE STOCK*. The policy was extended to multi-parts re-entrant systems by Yong (2001) and showed promising results.

We extended the work of Yong (2001) by studying the performance of CPP for three critical performance parameters i.e *lead times*, *standard deviation of lead times* and *waiting times*. Furthermore, Yong (2001) only considered the prioritized processing of parts under high demand and without specifying the policy parameters for bottleneck workstations. We also introduced a modified version of the policy for bottleneck workstations. Khalil, Stockton, and Ardon-Finch (2006) analyzed the performance of CPP for make-to-order environments. The policy showed good performance for small re-entrant systems in comparison to critical ratio. Khalil, Stockton, and Ardon-Finch (2008) determined the important parameters of the policy including hedging times and buffer sizes using genetic algorithms for small re-entrant systems. This paper extends the work of Khalil, Stockton, and Ardon-Finch (2006) and Khalil, Stockton, and Ardon-Finch (2008) by determining the policy parameters for a much larger system, i.e semiconductor fab line, introducing different

demand rates and product mix and comparing the performance of CPP with EDD, LS, and CR policies. (Kim et al. 1998) introduced new sets of dispatching and sequencing rules for reducing the mean cycle times while minimizing the tardiness values for products with different due dates. Chao Qi and Gershwin (2007) introduced *WIPLOAD* control rule for minimzing the *Lead Times* and *Standard deviation of Lead Times* for products with different priorities. Their lot release procedure was based on a pre-determined amount of inventory between workstations. Moreover, the lead times and the standard deviation of lead times were computed for products without the assignment of due dates for arriving parts, and with a product mix comprising of equal proportion of arriving orders. Our research included a system with finite buffer sizes, a mixed portfolio of products and a dynamic allocation of demands and due dates for arriving lots.

3 CONTROL POINT POLICY

Control point policy is a pull type control mechanism based on demand information in the form of due dates. The policy limits the entrance of a product into the system and further downstream based on two conditions that are executed on each part type. The part is first checked for surplus i.e how far ahead current production is as compared to its demand (or schedule). The second check is for the inventory i.e. a part is restricted to enter the system, or further downstream, if too much inventory of that part type already accumulate in the system.

3.1 Key Terms and Definitions

The key terminologies used in our research are described below:

- *Demand Lead Time* is refered to the time duration between the customer demand arrival and the due date of the demand
- *Service Rate* for a part type is the frequency of the parts reaching the finished goods buffer before or on due date
- *Manufacturing Cycle Time* is the time interval between when the lot is released in the system and the time when it reaches the finished good buffer. It does not include the time spent by the part in the finished goods buffer before being dispatched to customer
- *Throughput Rate/Production Rate* is the number of lots of products produced per unit time
- *Takt Time* is the time interval that must elapse between two consecutive units in order to meet the demand – it is based on monthly forecast for demand
- *Work-in-Process* includes all the material present in the system between the first machine and the finished good buffer – it does not include the material which is present in the raw material buffers
- *Waiting Time* is the summation of times, the parts spent in the buffers/queue waiting for their processing at the machines/work centers
- *Control Point* is any machine/work center where the control point policy is implemented
- *Hedging Times* is a conservative estimate of the remaining processing time of the part from the control point to the finished goods buffer
- *Availability* is a part selection criteria of CPP which requires a part to be present in the upstream buffer and have space in the downstream buffer to proceed after its processing at the machine
- *Readiness* is a part selection criteria in CPP that allows a part to be selected for processing once the sum of the current system time and the hedging time is greater than or equal to the due date of the parts

3.2 Time Based Policy

Gershwin (2000) introduced three versions of the policy, named as surplus based, time based and token based. In our research, we use the time based version of the policy, since we deal with the comparisons of due dates and expected remaining processing times of lots for parts selection in the semiconductor

fab lines, that are essentially the time based characteristics of the system. In addition to this, the system performance parameters including cycle times, standard deviation of cycle times and mean waiting times are also the time based metrics. Details regarding the surplus and token based versions can be found in Gershwin (2000).

Time based version of the CPP is used to evaluate the system characteristics on the basis of time. Due dates and hedging times are the comparison parameters governing the time based evaluation of parts in the system. The goal of the time based policy is to ensure that the parts reach the finish goods buffer close to its due date while minimizing the earliness and tardiness penalties. Hedging time is used to compute the performance of part with respect to its due date. Time based policy ensures that the parts reach the finish goods buffer close to the due dates while minimizing the earliness and tardiness penalties. The algorithm for time based version can be explained as follows:

Initialization Phase Parts are ranked on the basis of any priority scheme defined by the company. It may include most valuable clients, new products, inventory holding costs etc. Once the parts have been ranked, hedging times and buffer sizes for all the parts present in the system are calculated.

Execution Phase

Whenever a machine becomes idle (after completing an operation or repaired after a failure), a decision is made whether to operate it or wait. The execution phase of the algorithm consist of the following steps:

(a) Consider the lots that are *available*.
(b) Among the available lots, select those that are *ready*.
(c) Select the highest ranked work lot. Operate on the lot in the upstream buffer with the earliest due date.
(d) If no lots satisfy (b) then wait until the first lot does.

We follow the Gzouli (2000) for the part selection algorithm in the execution phase and it is presented in Figure 1.

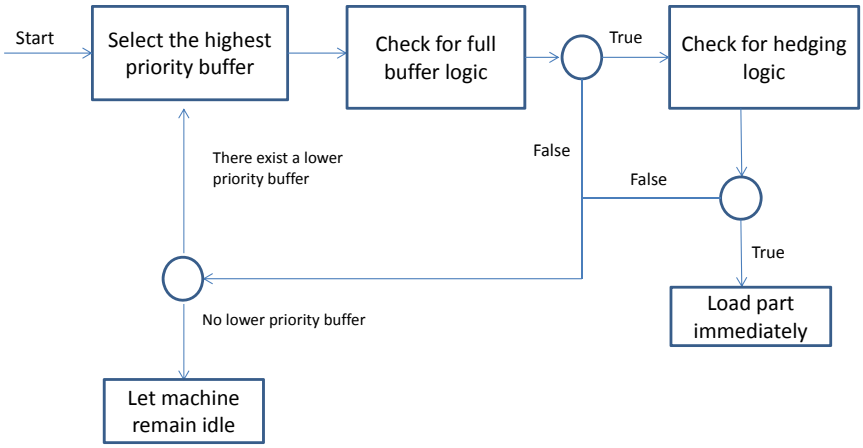

Figure 1: Part selection algorithm for CPP

4 SIMULATION MODEL

4.1 Wafer Fab Data

For our modeling and analysis of the semiconductor fab, we use the data, TRC FAB of HP, introduced by Wein (1988). Among the three fabs present in the TRC facility, fab 1 is selected for our analysis. That is,

the information about the mean processing times (MPT), mean times between failures (MTTF) and mean times to repairs (MTTR) for the workstations are found in Wein (1988). The objective of our research is to analyze the performance of the scheduling policies in the fab for multiple parts and therefore we need to have different part types with different processing steps. Unfortunately, the TRC FAB has only one part type. Therefore, we created two hypothetical part types with different processing steps. The information about the three part types A, B and C are available on our website (Talha Liaqat 2014).

4.2 Simulation Modeling Assumptions

The following modeling assumptions are used to carry out the simulation experiments. These assumptions are defined within the assumptions made with previous research including Wein (1988), Gzouli (2000) and Yong (2001).

1. A lot size comprises of 24 wafers
2. The time between demand follows exponential distribution
3. The lots are associated with their due dates at the time of arrival. The due dates for n^{th} part of type q is assigned on the basis of following relation

$$D_{nq} = d_{nq} + l_q,$$

   where d_{nq} represents demand arrival time and l_q is the demand lead time
4. The due dates allocation distribution is based on uniform distribution
5. Machines are assume to operate asynchronously – parts are loaded when the proper authorization as per defined algorithms for the scheduling policies
6. Machines only fails while operating – this is known as operation dependent failure
7. The mean processing time, mean times to failure, and mean times to repair for all the machines follow exponential distributions
8. There is no setup time when a machine is switching from one part type to another
9. All the scheduling policies operate under *blocking before service* algorithm – a part can only be loaded on the machine when there is space available in downstream buffer to which it can proceed after processing

4.3 Simulation Modeling

Discrete event modeling is utilized to simulate the behavior of semiconductor fab line. Event graph modeling formalism is used to develop the simulator for semi conductor fab lines since it studies the inter relations between the interacting elements. The event graph model developed for our research is presented in Figure 2. For the detailed notation of the event graph formalism, see Choi and Kang (2013).

The notation used in the event graph model are presented below:

- s: station number
- $Q(s)$:buffer Q at station d
- $M(s)$:machine at workstation s
- JT :job type
- $Route[j,p]$:process flow p of part type j
- $t[j,p]$:processing time of part type j at process step p
- $t_f(s)$:mean time to failure of workstation s
- $t_r(s)$:mean time to repair s
- $B(s)$:blocking condition checking variable at workstation s
- $Delay(s,ns)$:transporation time between two workstations s and ns

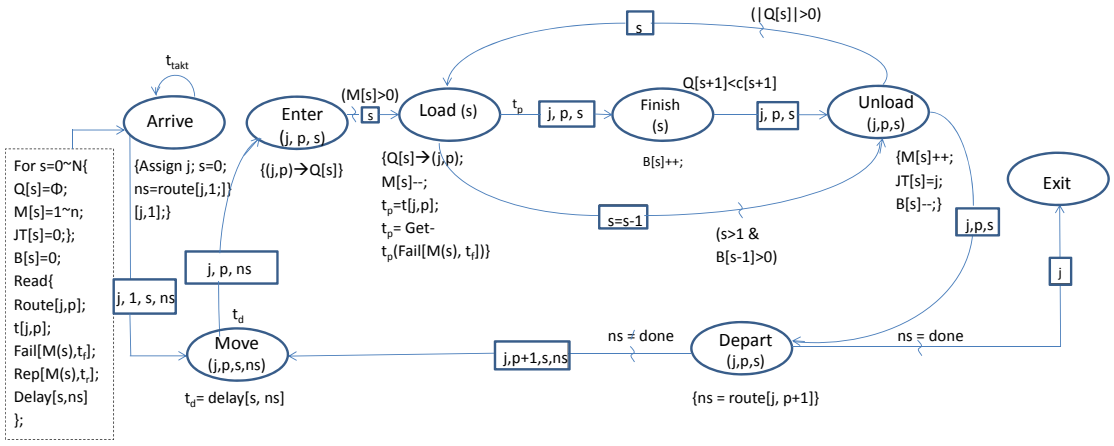

Figure 2: Event Graph Model for the Simulator

The square shapes in Figure 2 represent the parameters for the model, whereas the oval shapes represent the event nodes. The delay time between workstations is assumed to be 0. The initialization stage consists of setting all the machines in the available state with both upstream and downstream buffer levels set to 0. The job is identified by its process flow and due date at the *arrive* event. Each new lot enters the system after a *TAKT* time of t_k based discretionary input control mechanism, which in our case is the comparison of hedging times and due dates. The job is transported to the first station in its processing at the *move* event. The job queues up in the upstream buffer at the *enter* event. All the lot sequencing rules are implemented at the *enter* event. The *load* event represents the workstation/machining center, where the lots are processed as per their predefined processing times. Once the processing of the job is completed, it is offloaded from the machine at the *unload* event. The job is then transported to the next workstation through the *move* event. In case the job completed its all processing steps, it moves out of the system. The system statistics including mean cycle times, work in process and waiting times etc. are updated for each job departure from the system. All the machines in the system are subjected to failure as per their mean times between failures (MTTF). The failed machines are repaired as per their mean time to repairs (MTTR). The simulation modeling is validated by comparing its performance with smaller re-entrant lines introduced by Gzouli (2000), Yong (2001), and Jang (2007), prior to being implemented for semiconductor fab lines.

4.4 Scheduling Policies Characteristics

This section discuss the characteristics of the four scheduling policies used in this research.

4.4.1 Control Point Location

Control point represents the workstation/machine where CPP is implemented. The cleaning work center (work station 1) is chosen as a control point in our research. The station is significant in controlling the flow of parts in the system since it represents the first processing step for all the part types, a point where the disorderly mingling of parts types is high and a place where the lots return for cleaning after each layer of deposition on the wafers. This station is also the third most revisited station for the parts. The simulation experiments are executed by implementing CPP at multiple workstations such as station 22, 23 and the bottleneck workstation 14.

4.4.2 Priority Scheme

For control point policy, if a lot P_1 is at process step i_1, a lot P_2 is at process step i_2 at the same control point and $i_1 > i_2$, then P_1 has a higher priority than P_2. However if $i_1 = i_2$ then the priority is determined based on the product type. For EDD, CR and LS policies, lots are selected on the basis of due dates, critical ratios and minimum slacks.

4.4.3 Hedging Times

Hedging times represent the conservative estimates of the amount of remaining processing times from the control point to the finished goods buffer. It also includes the time parts spend in buffers, repair times, and transportation time between workstations.

Preliminary simulation experiments are conducted to determine the values of waiting times of parts in the system with FIFO rule. It is observed that parts spent 80 percent of their cycle times waiting in queues. Therefore hedging times for part type j at process step is determined on the basis of the following relation:

$$H_{ij} = \Sigma 5 \xi_{ij},$$

where ξ_{ij} represents the expected processing times of part type j at process step i

4.4.4 Buffer Sizes

Control point policy limits the cumulative amount of inventory between each pair of control points. The total inventory between each pair of control points is calculated by the following relation:

$$\frac{HT(s,j) - HT(s+1,j)}{T_j},$$

where *HT(s,j)* represents the s^{th} visit of part type j to the control point workstation and HT(s+1,j) represents the $(s+1)^{th}$ visit of the same part type to the control point workstation. Preliminary simulations are conducted to determine the average inventory levels between the workstations. Based on the preliminary results, the cumulative inventory between each pair of control points is distributed among the buffers. For ensuring a fair analysis, the same buffer sizes are used for all the policies tested.

5 SIMULATION EXPERIMENTS

A total of 10,000 simulation experiments are conducted. Replications of the simulation experiments are conducted to ensure the achievement of half length of 95 percent confidence interval, divided by the output of interest is less than 3 percent. In this case, the output is said to have a relative error of less than 3 percent. (Hammersley and Handscomb 1991) provides a good discussion of statistical analysis using relative errors.

The fab is simulated long enough to generate steady state results.

5.1 Performance Measures

With the simulation experiments, each policy is analyzed with the following performance measures:

1. Mean and standard deviation of cycle times
2. Mean waiting times and inventory levels (both in process as well in finished good buffer)
3. Service rates for the lots together with the implementation of finite size buffers and a non-uniform product mix

Table 1 presents the input parameters used for the simulation experiments.

Table 1: TRC Wafer Fab Information.

Product Type	A	B	C
Proportion	25 Percent	40 Percent	35 Percent
No of Processing Steps	172	163	190
Average Takt time, t (hrs)	4.1	2.7	3
Total Processing time/lot	545	537	581
Longest Processing Workstations	PLM6(13.88 hrs)	PLM6(13.88 hrs)	PLM6(13.88 hrs)

5.2 Simulation Results

Simulation experiments are conducted by implementing CPP at different workstations . For Set 1 experiments, CPP is implemented at workstation 1 and its performance is compared with EDD, MS and CR policies. The results of Set 1 experiments are set as benchmarks for assessing the improvement in systems performance when CPP is implemented at other workstations. For Set 2 experiments, CPP is implemented at workstations 22 and 23 along with workstation 1. For Set 3 experiments, CPP is modified and implemented at a bottleneck workstation 14 along with workstation 1. For all the three sets of experiments, Part A is given the highest priority, followed by part B with Part C being the least important. The parameters studied in the simulation experiments include mean cycle times (CT), standard deviation of cycle times (SDCT), mean waiting times (WT), work in process (WIP) and service rates (SR).

5.3 Set 1 Experiments

The CPP was implemented at *work station 1*, named as the *cleaning work center*. This work center was chosen to be a control point, since it is the first processing step for all the three part types, third most visited station and a point where disorderly mingling of parts was high.

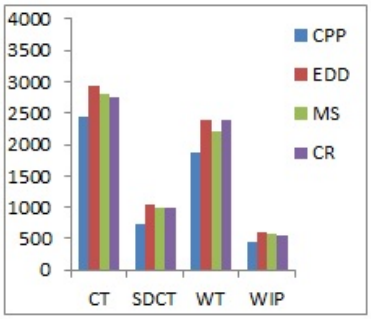

Figure 3: Policies Comparison for Product A, CPP at Station 1.

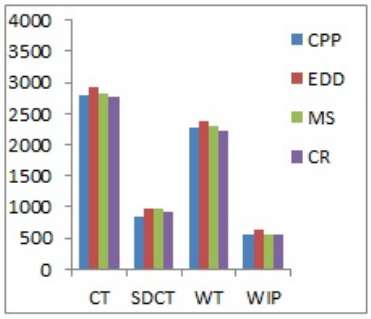

Figure 4: Policies Comparison for Product B, CPP at Station 1.

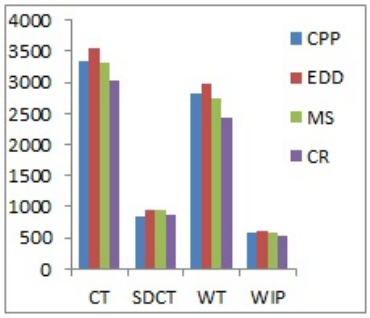

Figure 5: Policies Comparison for Product C, CPP at Station 1.

Figures 3, 4 and 5 show the performance of the policies for products *A*, *B* and *C* respectively. For the highest ranked product i.e. *product A*, CPP gave the best performance in terms of all the performance measures, followed by CR and MS. The EDD policy gave the worst performance among the four. For part 1, CPP showed an improvement of 11, 13 and 21 percent for mean cycle times in comparison to CR, MS and EDD policies respectively. The most valuable part can be a new product for the company, or a product with the highest profit margin etc. CPP also showed a good performance of work in process for *part A* with an improvement of 18 , 22 and 34 percent as compared to CR, MS and EDD Policies for part type A. An improvement of all these parameters was also accompanied by the improvement of service rates as shown in Table 2. In addition to this CPP showed minimum standard deviation of mean cycle times for all three part types. The CPP gave the second best performance after CR rule for *product B* for all the performance

parameters, whereas for *Product C*, it gave the third best performance. These results supported our claim for CPP performing the best when often there are priorities for part types often with similar characteristics such as due dates.

Table 2: Comparison of Scheduling Policies for Part A.

	TT	WT	WIP	SR
CPP	2430	1885	457	0.875
EDD	2941	2396	614	0.784
MS	2814	2197	587	0.802
CR	2742	2392	562	0.818

5.4 Set 2 Experiments

The analysis of WIP levels in Set 1 experiments showed an excessive inventory accumulation for work stations 22, 23 and the bottleneck work station 14 (with the highest level of inventory). Therefore, workstations 22 and 23 were selected to be the control points locations along with work station 1 to analyze the improvement in the performance of the system. Figures 6, 7 and 8 show the performance of the policies with CPP implemented at workstations 1, 22 and 23.

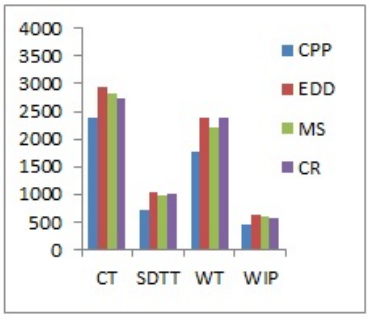

Figure 6: Policies Comparison for Product A, CPP at Station 1,22,23.

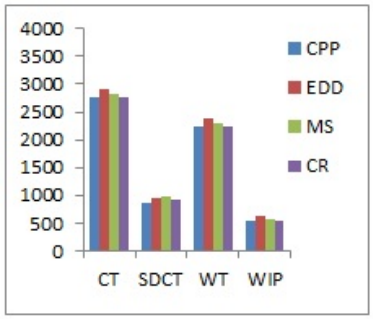

Figure 7: Policies Comparison for Product B, CPP at Station 1,22,23.

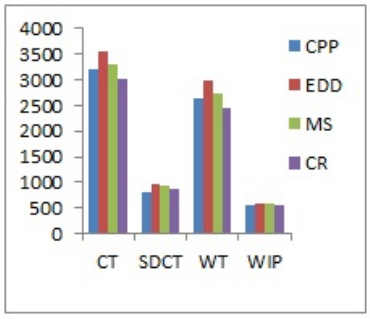

Figure 8: Policies Comparison for Product C, CPP at Station 1,22,23.

For part A, CPP showed again showed the best performance for all the performance measures. The performance for the other policies for all the part types were the same as compared to Set 1 experiments. The purpose for conducting the Set 2 experiments was to analyze the improvement in CPP performance, when CPP is implemented at more than one workstation. Results show an improvement of 13, 15 and 18 percent for mean cycle times in comparison to CR, MS and EDD policies respectively for part type A. The CPP also showed an improved performance of work in process levels and waiting times. The performance of parts B and C also improved in comparison to the results obtained in Set 1 experiments. Both parts showed an improvement in service rates from 0.75 to 0.80 and 0.72 to 0.75 respectively.

5.5 Set 3 Experiments

Previous studies on the performance analysis of semiconductor fab lines showed that the improvement in semiconductor fab lines is largely dependent on the performance of the bottleneck workstations. Several scheduling policies have been used to improve the throughput rate and utilization of the *bottleneck* workstations like work *load regulating , closed loop, starvation avoidance* etc. Workstation 14, the photolithography workstation is the bottleneck station for the fab line analyzed for our simulation experiments. Therefore workstation 14 was selected as a control point along with work station 1. For the bottleneck workstation,

the execution algorithm of CPP was modified in a way that the hedging times for all the parts were assumed to be infinite. As this way, we ensured that the bottleneck machine became never starved. All the other characteristics of the policy including the ranking criteria and the availability logic were the same.

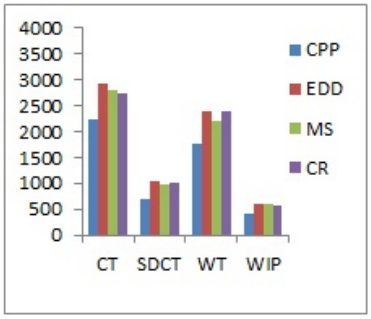

Figure 9: Policies Comparison for Product A, CPP at Station 1,14.

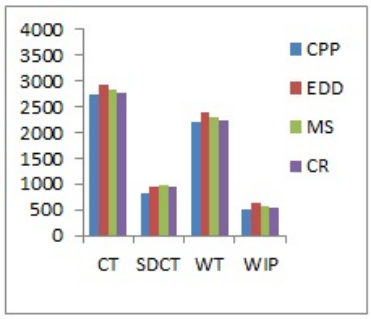

Figure 10: Policies Comparison for Product B, CPP at Station 1,14.

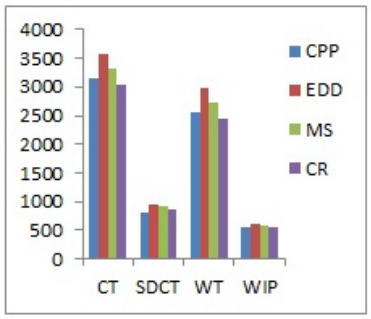

Figure 11: Policies Comparison for Product C, CPP at Station 1,14.

The results of Set 3 experiments are shown in figures 9, 10 and 11. Again for Part A, CPP gave the best performance in comparison to other scheduling policies. The cycle times for part type A showed an improvement of 18 , 20 and 26 percent improvement in comparison to CR, MS and EDD policies respectively. The mean waiting times and inventory levels were also the minimum as compared to other policies. Set 3 experiment showed the best performance for the part type A as compared to the first two sets of experiments. Moreover, CPP also showed the best performance for part type B for all the performance parameters, with the second best performance shown by CR, with EDD Policy giving the worst performance. These results supported our claim of CPP giving the best performance for prioritized parts while maintaining a balance for the other parts. The results indicate that a good combination of *input control* and *lot sequencing rules* at the bottleneck station improved the system performance significantly as compared to the controls implemented at the non bottleneck stations.

6 CONCLUSION AND FUTURE RESEARCH

We introduced control point policy (CPP) and discussed its implementation for multiple parts , multi process, re-entrant semiconductor fab line. We extended the previous work done on CPP Policy by implementing it with prioritized parts with low demand rates and implementing it for multiple workstations including the bottleneck workstation. The most important characteristic of the CPP is its ability to produce the prioritized parts with minimum cycle times and inventory levels. The policy not only gave good performance for prioritized parts but also gave the best balance performance for non-prioritized parts. This implies that as the number and types of products increases, CPP can give a far better performance in comparison to other policies. Since the CPP is a new policy so there are a lot of potential areas for improvement. Our ongoing research includes development of set of rules for optimal selection and location of control points and methods for dealing with batching operations since many operations in the fab like diffusion involves batching of different part types. Other areas of potential improvement include implementation of the CPP for parallel workstations with different processing speeds for maximum equipment utilization and for situations where lots have different processing times for each visit to a particular workstation.

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AUTHOR BIOGRAPHIES

TALHA LIAQAT received his Bachelors degree from University of the Punjab. He is currently a Masters Student in Systems Design and Management Lab, Korea Advance Institute of Science and Technology. His research interest include production planning and operations scheduling in flexible manufacturing systems His email address is talha@kaist.ac.kr.

YOUNG JAE JANG received his Ph.D. degree in mechanical engineering from Massachusetts Institute of Technology (MIT) in 2007 and a double M.S. degree in mechanical engineering and operations research from MIT in 2001. He received a B.S degree in aerospace engineering from Boston University in 1997. He is currently an Assistant Professor in the Industrial and Systems Engineering Department at the Korea Advanced Institute of Science and Technology (KAIST), South Korea. His current research includes stochastic modeling of complex systems and optimizations in transportation and logistics systems. Before he joined KAIST, he worked at Micron Technology, Inc., VA, USA, the global semiconductor chip provider, where as project manager, he led a global initiative to improve the efficiency of the manufacturing facilities located worldwide. While working at Micron, he was also involved in activities supporting the company's operational and strategic decision making using quantitative modeling and analysis techniques. His email address is yjang@kaist.ac.kr.