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WORKLOAD CONTROL MECHANISMS AND SCHEDULING IN SEMICONDUCTOR MANUFACTURING REVISITED

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ABSTRACT

Despite the recent advances in rule based workload control (WLC) mechanisms, recent semiconductor literature has neglected them, although it was shown that they outperform most other periodic and continuous order release models. Therefore, this paper compares the most widely used and considered best performing WLC models: the LUMS-COR, with its equivalent from the semiconductor literature, the Starvation Avoidance (SA) method in combination with different scheduling rules. We compare the performance of these approaches by using a simulation model of a scaled-down wafer fabrication facility. The results show that the LUMS-COR outperforms the SA model with regard to total costs and timing measures. In comparison, the LUMS-COR model releases orders later which reduces the holding costs of finished goods inventory (FGI) and yields only slightly higher average shop floor time and lateness measures.

1 INTRODUCTION

WLC originated from the idea to control flow times by controlling order releases and thus the level of work-in-process (WIP) and output (Kingsman et al. 1989; Wiendahl 1995). An order release model has to decide which unreleased orders should be sent from a pre-shop pool to the shop floor, where the pre-shop pool seeks to smooth out fluctuations in the incoming flow of orders. Within WLC literature, rule based order release mechanisms determine when to release orders by employing a set of rules (Bergamaschi et al. 1997) and by choosing different parameter settings (Glassey and Resende 1988; Wiendahl 1995). However, despite recent developments in WLC literature which mainly focuses on Small and Medium Enterprises in Make-To-Order environments (Thuerer et al. 2012), recent research on semiconductor manufacturing has not taken advantage of these developments, in particular the LUMS-COR method introduced by Thuerer et al. (2012). Consequently, this papers' contribution is twofold: (1) it serves as a bridging paper between two largely separately developed streams of research and (2) it analyzes whether the LUMS-COR approach improves the performance of semiconductor wafer fabs. Moreover, there has been extensive literature on the relation between order release and scheduling and thus, we include three scheduling rules in our analysis.

2 SIMULATION MODEL AND EXPERIMENTAL DESIGN

We use a simulation model of a re-entrant bottleneck (BN) system which was built with attributes of a real-world semiconductor wafer fab previously studied in WLC research (Kayton et al. 1997). The simulation model is made up of 11 work centers (WC), each with one server except the BN that has two servers. The processing times for the WC are log-normally distributed, the inter-arrival times of orders are normally distributed, three products (product mix equals $3:1:1$) are produced and the demand was set to yield 90% BN utilization. There are two WC with low reliability which can starve the BN due to poor

availability and the model has batching WC early in the process. The considered release mechanisms are: (i) Immediate Release (IR), (ii) Starvation Avoidance (SA) which is a purely continuous release mechanism and focuses on releasing new orders whenever the sum of the direct load and the indirect load of the BN drops below a pre-determined level (Glassey and Resende 1988; Fowler et al. 2002), and (iii) LUMS-COR which is a hybrid approach incorporating a periodic, load-based release element, i.e. orders are only released if workload norms are not violated, and a continuous element which tries to avoid starvation at idling WC (Thuerer et al. 2012). For a summary of the experimental design see Table 1.

Table 1: Experimental Design.

Order Release	**Dispatching**	**Tested Parameters**
Immediate Release (IR)	FIFO, SRPT, SA	for FIFO and SRPT: - / for SA: α (2, 3, 4, 5, 6)
SA	FIFO, SRPT, SA	α (2, 3, 4, 5, 6)
LUMS-COR	FIFO, SRPT, SA	α (2, 3, 4) norm (1,000, 1,100, 1,200, 1,300, 1,400)

The period length was set to 1,440 minutes, each scenario was replicated 80 times, the warm-up phase was set to 100 and data was collected over 900 periods. The main performance measure are total costs which consist of the WIP, FGI and backorder costs over all periods where we set the cost parameters in the relation: $2\frac{1}{3} : 1 : 3\frac{1}{3}$ similar to earlier WLC studies in semiconductor industry (Albey and Uzsoy 2015).

3 RESULTS

Regarding scheduling, FIFO is the best (in terms of total costs) dispatching rule for all but the SA order release mechanism which yields the lowest costs with SA dispatching. In numbers, the best SA scenario yields \$18,307.96 and the best IR scenario yields \$30,591.31 higher average costs compared to the best LUMS-COR model. More precisely, the best LUMS-COR scenario yields significantly less costs by releasing orders later which results in less FGI costs. At the same time, the mean lateness of the best LUMS-COR scenario is only about 118 minutes higher and only about 4.75% more orders are tardy in comparison to the other models which is negligible, considering that the LUMS-COR model releases orders on average more than one and a half periods (2,268.44 minutes) and more than two and a half periods (3,679.94 minutes) later than the best performing SA and IR model. Likewise, the difference between shop floor times is significant, but low in absolute numbers: For LUMS-COR, the orders take on average 300.68 minutes and 355.99 minutes longer to traverse through the system in comparison to SA and IR.

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